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Gateway Clocks

Delivering Precise Robust Synchronization

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WSTS: April, 2013

Agenda

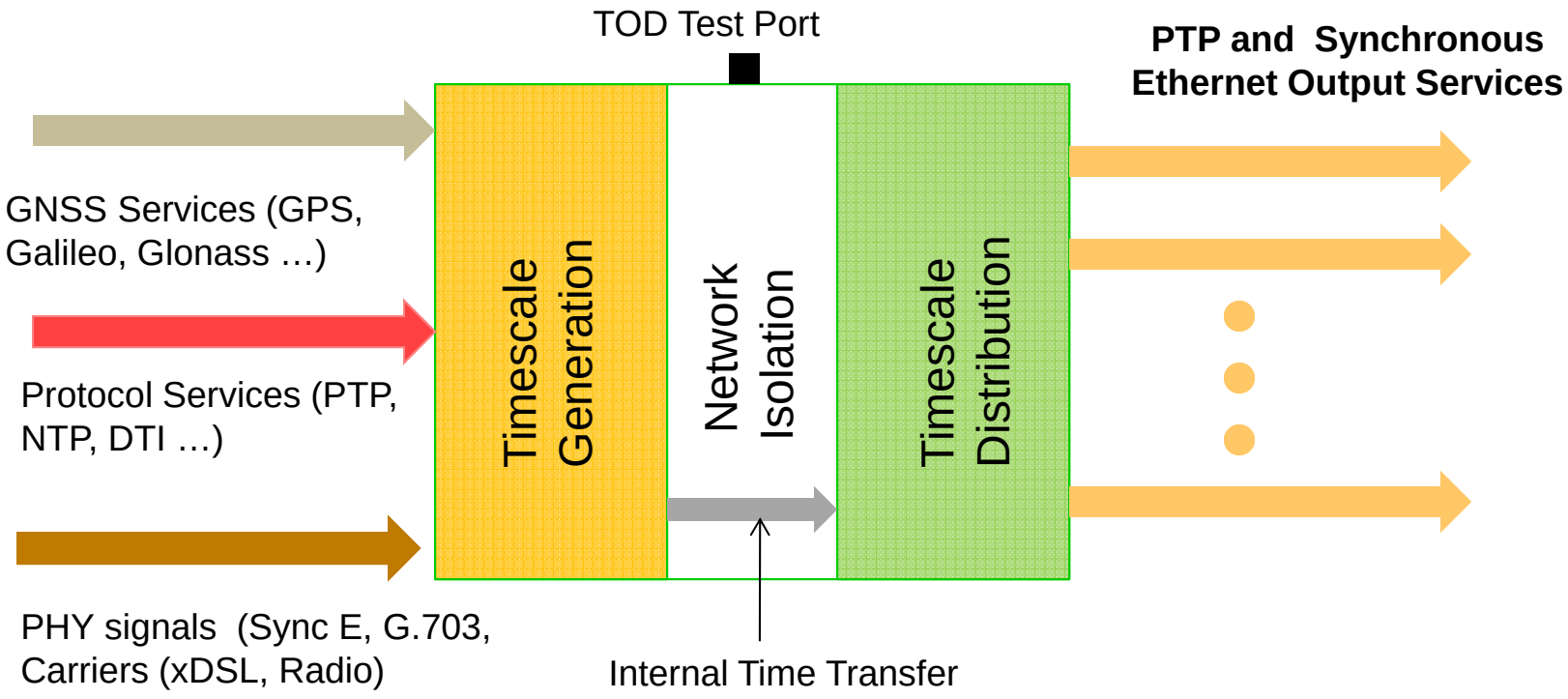
Gateway Clock Description

Phase/Time Service Delivery

PTP with Automatic Path Delay Compensation

Summary

Gateway Clock Functional View



Gateway Clock- Multiple Control Planes

- A gateway clock generates traceable time and frequency outputs :
  - •Source for Time Control can be different than Frequency Control
  - •The frequency control plane stabilize the local oscillator to support enhanced time control.
  - •Frequency and Time control operate simultaneously
  - •Traceability Control mitigates path asymmetry
- Practical examples of network inputs are shown. Of course basic operation with single input is an option.

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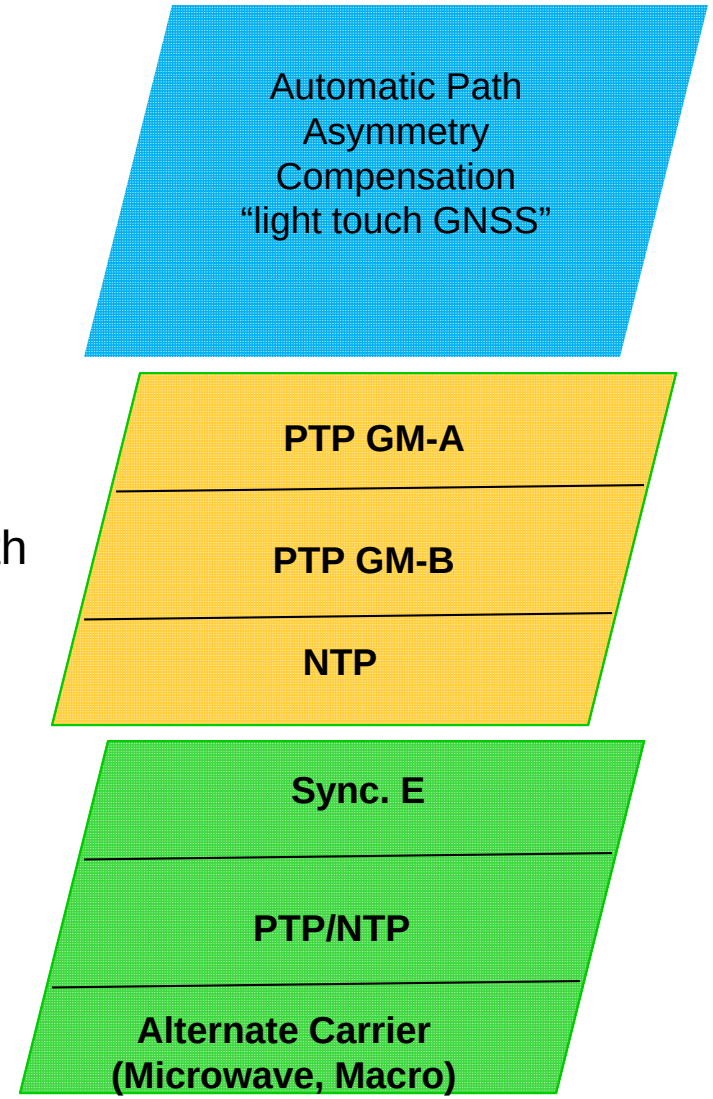


Why Automatic Path Asymmetry Compensation ?

The fundamental issue of asymmetry is captured in both the original 1588v1 standard (2002) as well as the subsequent release 1588v2 in 2008.

Excerpts from IEEE 1588-2002

The following assumptions must be met to achieve optimal clock synchronization performance: (6.1.3)

— Network delay between master and slave on a subnet must be symmetric (see 7.8.1.2).

This computation assumes that the path lengths are identical in the two directions. If additional knowledge is available concerning any possible path asymmetry, this computation shall be corrected so that the value of (one_way_delay) more accurately represents the time of propagation of a Sync message from the master to the slave clock. (7.8.1.2)

- Section 6.2 Principle assumptions about the network and implementation recommendations

Like all message-based time transfer protocols, PTP time accuracy is degraded by asymmetry in the paths taken by event messages; see 7.4.2. Specifically the time offset error is 1/2 of the asymmetry. (6.2)

Asymmetry is not detectable by PTP; however, if known, PTP corrects for asymmetry. (6.2)

Asymmetry can be introduced in the physical layer, e.g., via transmission media asymmetry, by bridges and routers, and in large systems by the forward and reverse paths traversed by event messages taking different routes through the network. Systems should be configured and components selected to minimize these effects guided by the required timing accuracy. In single subnet systems with distances of a few meters, asymmetry is not usually a concern for time accuracies above a few 10s of ns. (6.2)

Why Automatic Path Asymmetry Compensation ?

Excerpts from IEEE 1588-2008

Excerpt from IEEE 1588-2008 Section 6.6.3 Synchronizing ordinary and boundary clocks

The computation of offset and propagation time assumes that the master-to-slave and slave-to-master propagation times are equal. Any asymmetry in propagation time introduces an error in the computed value of the clock offset. The computed mean propagation time differs from the actual propagation times due to the asymmetry. (6.6.3)

Asymmetry effects are not limited to delay mechanisms only on the switches and routers asymmetry will be introduced in the physical layer.

Any asymmetry in the propagation times t-ms and t-sm introduces an error into the computed value of the link delay. (6.6.4)

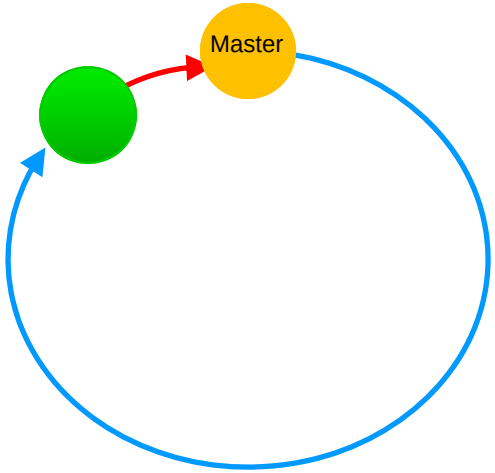
The overarching issue of asymmetry is the focus of the next section. It defines a correction term (delay_asymmetry) with the conclusion that measuring this term is beyond the scope of the IEEE 1588 standard.

Messages from master to slave and slave to master shall traverse the same network path in any system containing two-step clocks on such paths. Messages from requestor to responder and from responder to requestor shall traverse the same network path in any system containing two-step clocks on such paths. They should traverse the same path in all systems to minimize asymmetry.

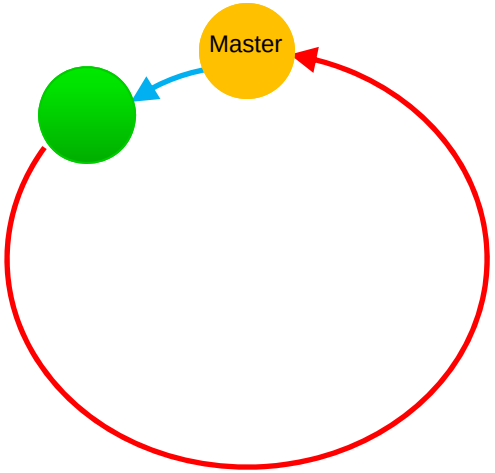
The measurement of delay_asymmetry is out of scope of this standard. (7.4.2)

Limits of asymmetry error

Case A: Long Forward Path and Short Reverse Path. Under Estimate Forward Delay using (Round-Trip-Delay/2). Worse Case Slave Time behind Master by (RTD/2)



Case B : Short Forward Path and Long Reverse Path. Over Estimate Forward Delay using (Round-Trip-Delay/2). Worse Case Slave Time ahead Master by (RTD/2)



Note: Asymmetry Error directly proportional to Round Trip Delay
Delivery Time Traceability limited by Round Trip Delay

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Gateway Clock Description

Phase/Time Service Delivery

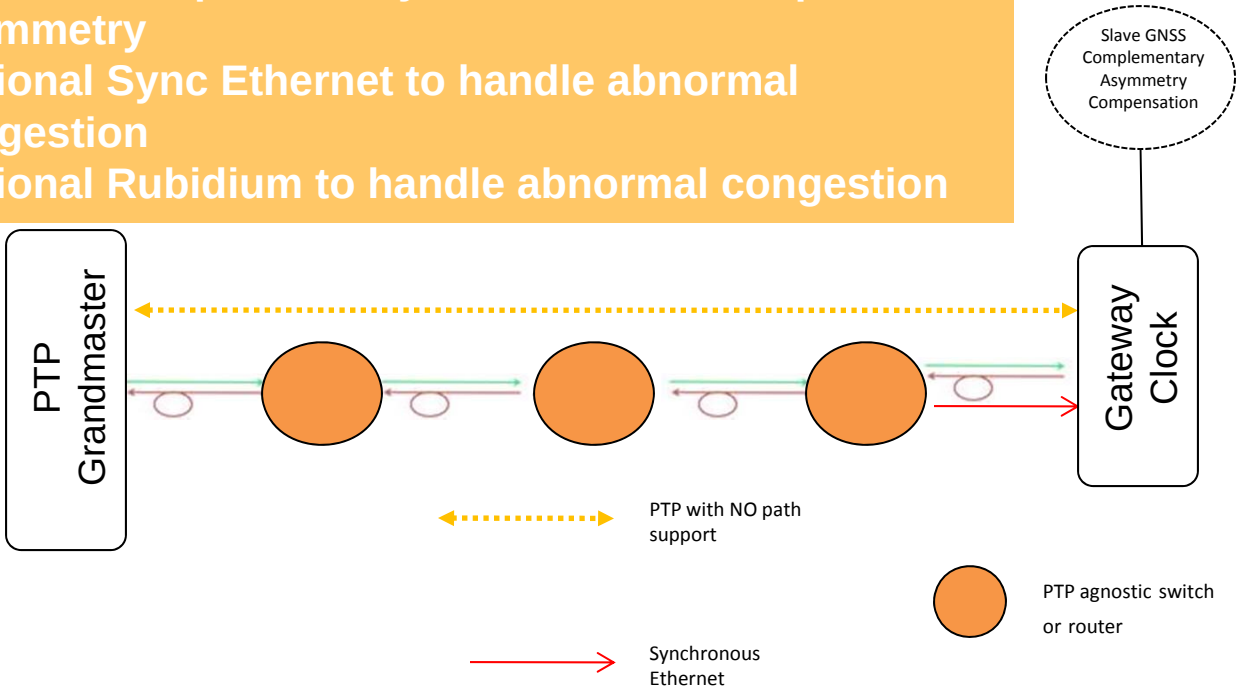
PTP with Automatic Path Delay Compensation Example

Summary

Phase Delivery Today with PTP

Service Delivery will require no on path support:

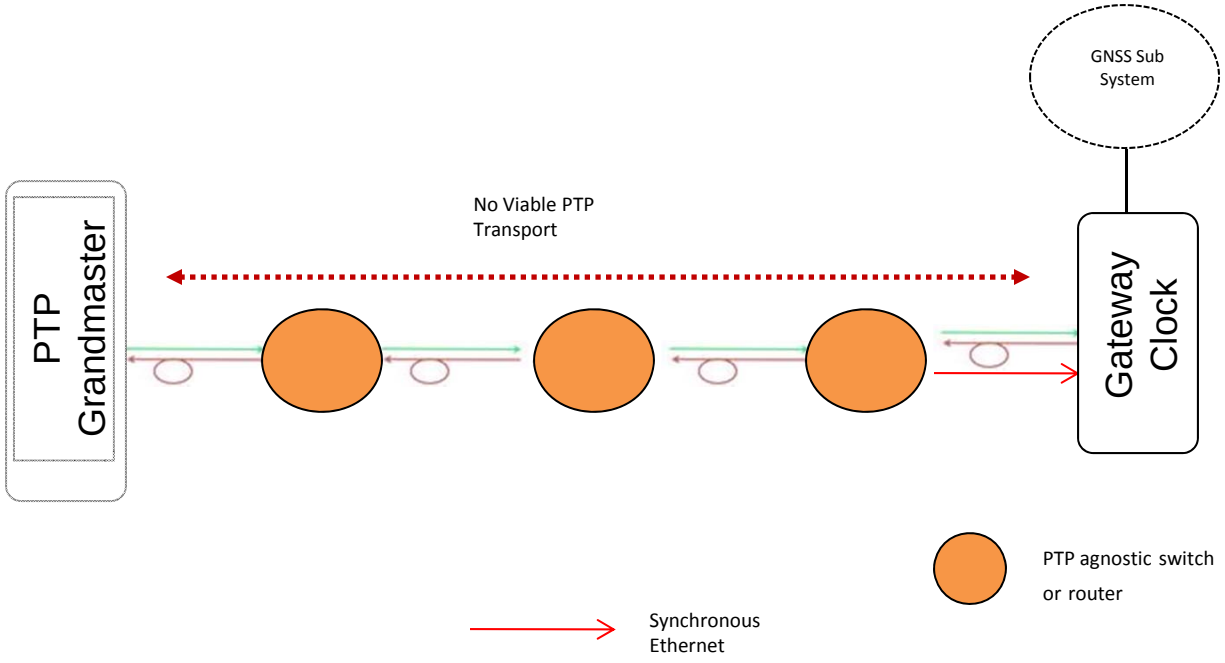
1. PTP without on-path support or partial support
2. SC 2.x Sub-Microsecond Phase Delivery documented over multiple G.8261 test environments and other key transports
3. Optional complementary GNSS to remove path asymmetry
4. Optional Sync Ethernet to handle abnormal congestion
5. Optional Rubidium to handle abnormal congestion



Service Delivery Today (No PTP)

Service Delivery is GNSS based:

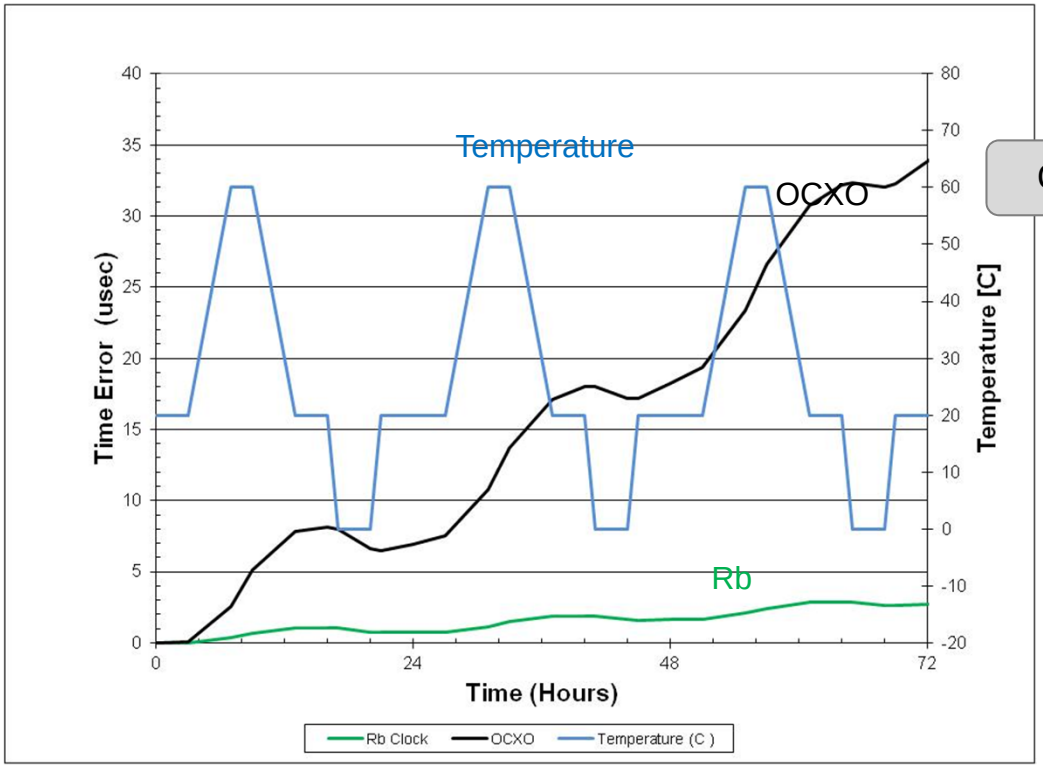
1. **Transport unsuitable for phase (xDSL)**
2. **GNSS primary source of traceability**
3. **Optional Sync Ethernet extends time holdover**
4. **Optional Rubidium extends time holdover**



Holdover Protection

Holdover: *continuous operations when primary synchronization source is lost*

Rubidium
< 1.5 µs per 24 hrs



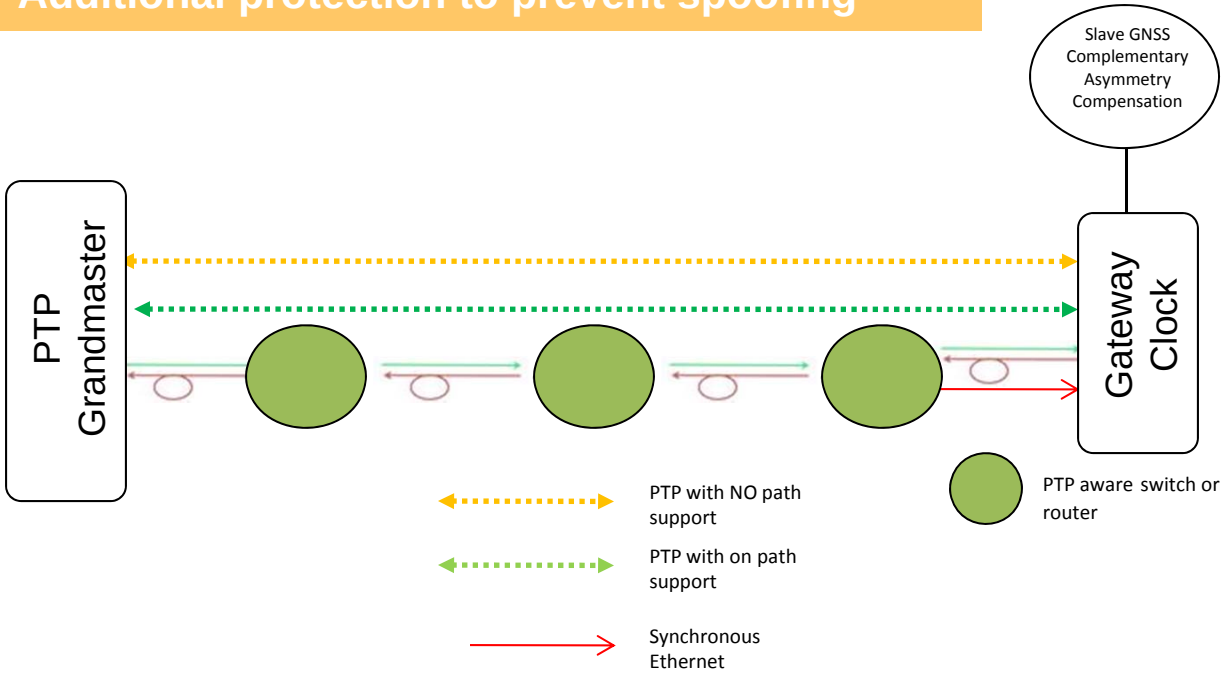
OCXO 8 µs per 24 hrs

Rubidium in macro eNodeB to support +/- 1.5 µs for 24 hrs.

Service Delivery Future

Service Delivery with on path support:

1. **PTP without on-path support flows are still fully supported**
2. **On path support can be verified and protects against failures of BCs or TCs**
3. **Additional protection to prevent spoofing**



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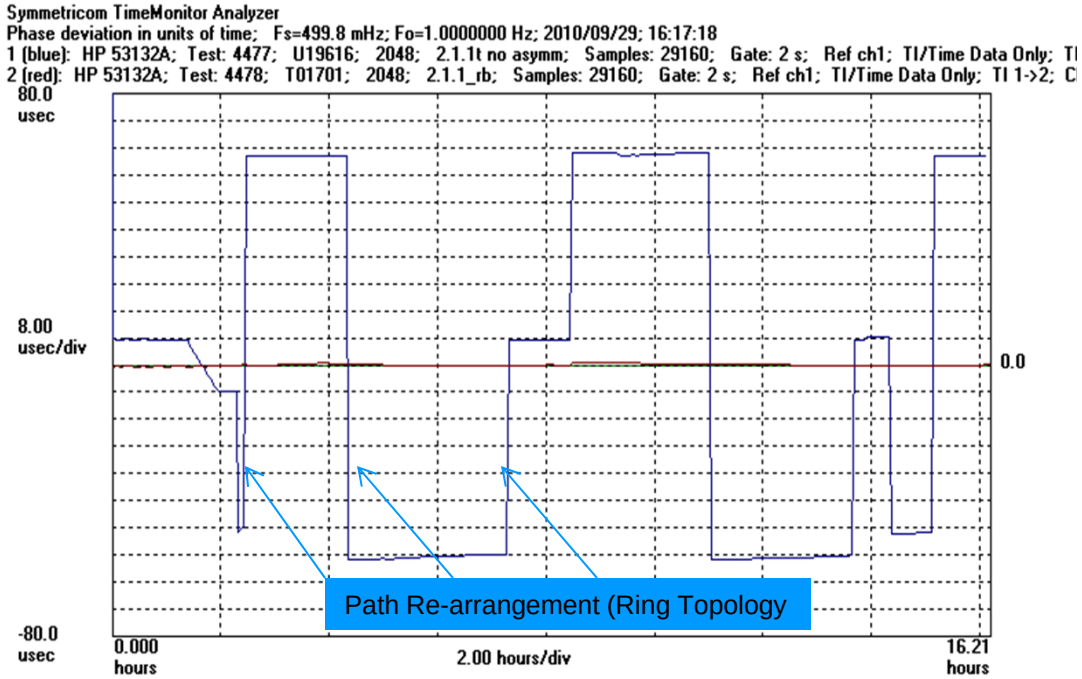
PTP with Automatic Path Delay Compensation

Summary

Using GPS/GNSS to Learn PTP Asymmetries

- **Asymmetry Correction Algorithm supplies external correction factor defined in 1588 standard.**
- **Algorithm learns asymmetries to prevent in-accurate time output**
- **Traceability Control Plane allows for intermittent poor reception operation including jamming**

  (“light touch GNSS”)

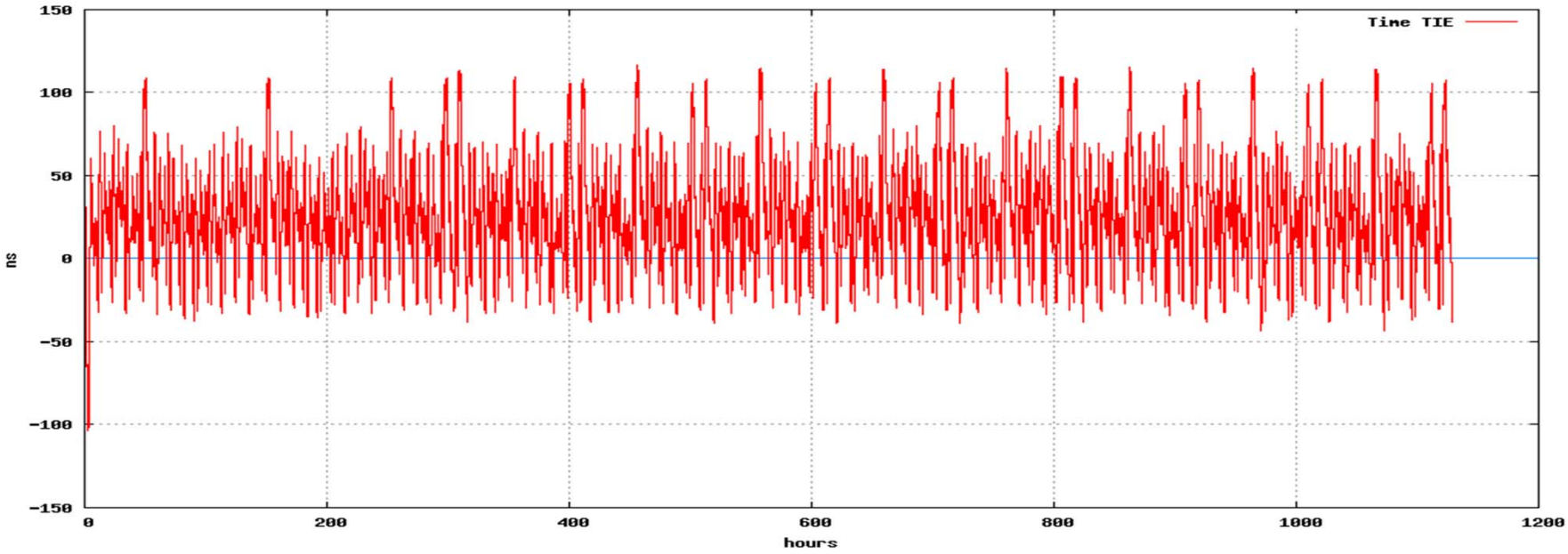


Performance on Customer Network test environment:

BLUE: PPS Performance without Asymmetry correction.

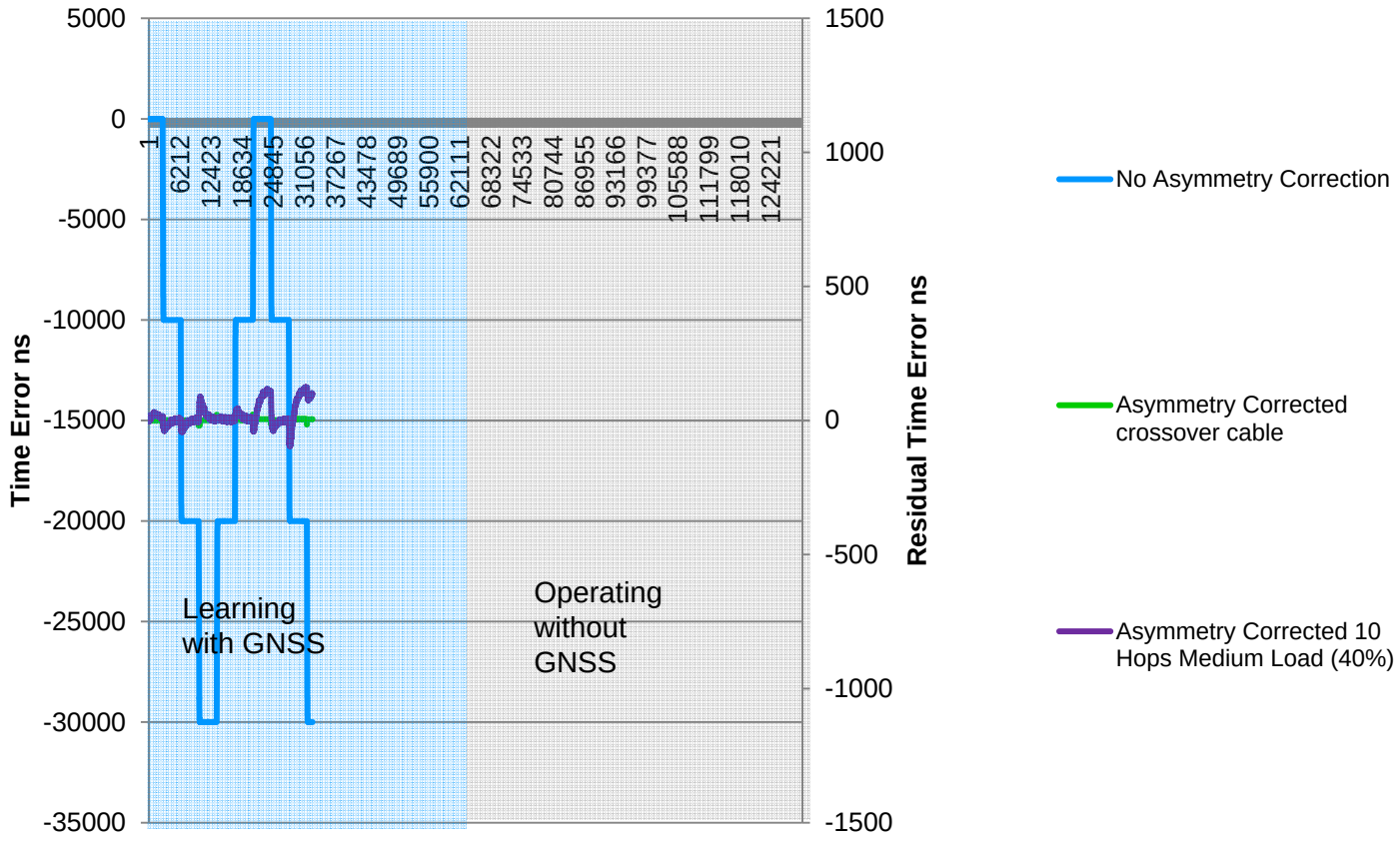
RED: PPS Performance with Asymmetry correction.

Automatic Path Delay Compensation Long Term (45 days)

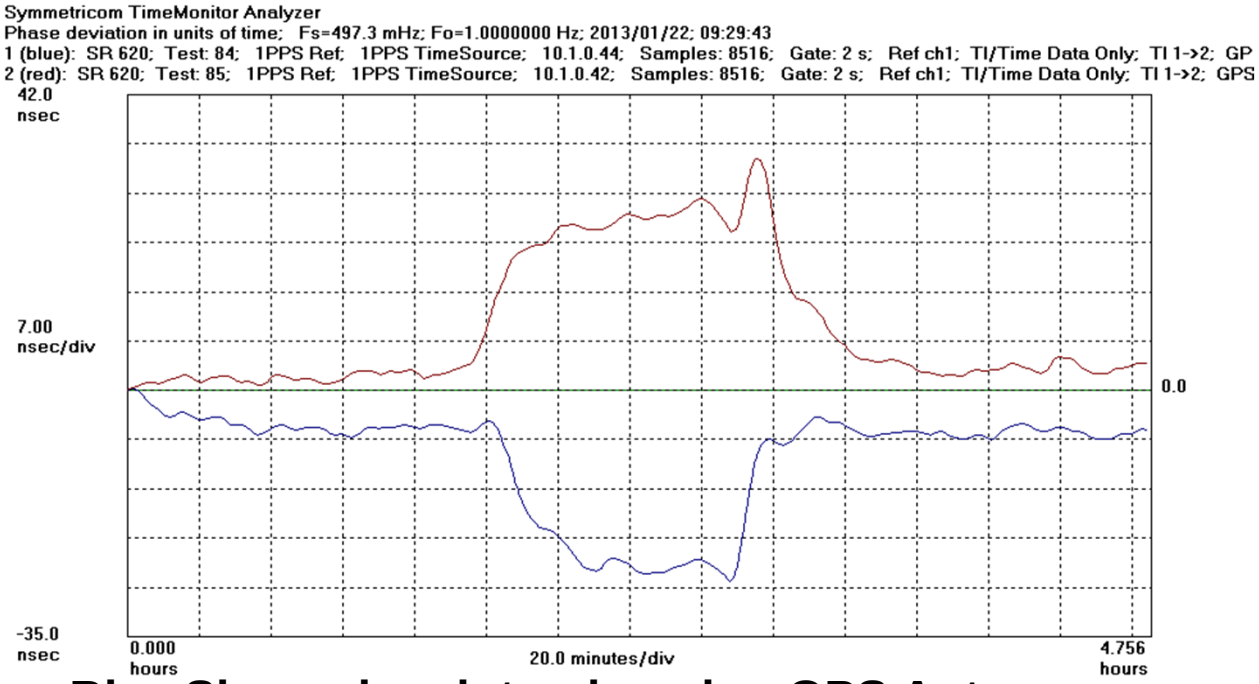


- Performance based on playback of Customer Network captured packet delay variation including rearrangement transients.
- PTP over Ethernet over SDH (2 rings Ring 1 16 nodes , Ring 2 4 nodes)
- 90 path rearrangement events during test.
- Accuracy better than125ns after warm up.

Automatic Path Delay Compensation Learning Behavior



GPS Antenna Group Delay Bias Effects



Bias Skew when interchanging GPS Antenna

The Bottom Line …

- Gateway Clock provides operators required flexibility to provide needed timing services at the edge as PTP matures.
- Gateway Clock operating with traceability control provides a real world solution to path asymmetry challenges.
- Gateway Clock utilization of multiple inputs provides robust solution
  - PTP time outage performance is unaffected by the use of lower cost, power and size oscillator technology.
  - Automatic Path Asymmetry correction can be accomplished with “Light Touch GNSS”

Thank You

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Concept of a Clock as a Phase/Time/Frequency Service Gateway

Some useful concepts from Wikipedia:

- In telecommunications, the term **gateway** has the following meaning:
  - In a communications network, a network node equipped for interfacing with another network that uses different protocols.
    - A gateway may contain devices such as protocol translators, impedance matching devices, rate converters, fault isolators, or signal translators as necessary to provide system interoperability. It also requires the establishment of mutually acceptable administrative procedures between both networks.
    - A protocol translation/mapping gateway interconnects networks with different network protocol technologies by performing the required protocol conversions.
  - Gateways, also called protocol converters, can operate at any network layer. The activities of a gateway are more complex than that of the router or switch as it communicates using more than one protocol.

PTP with Sync. Ethernet Time Performance during 8 hour PTP Outage

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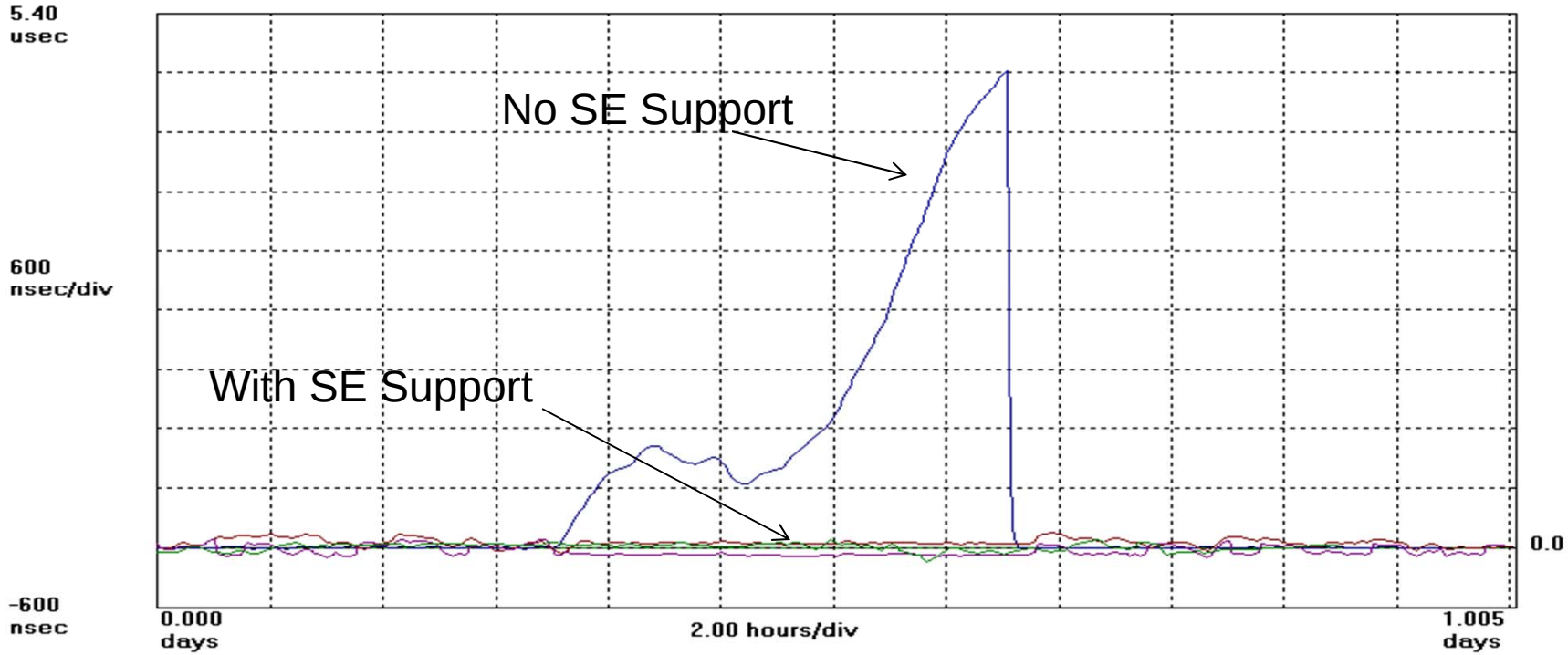
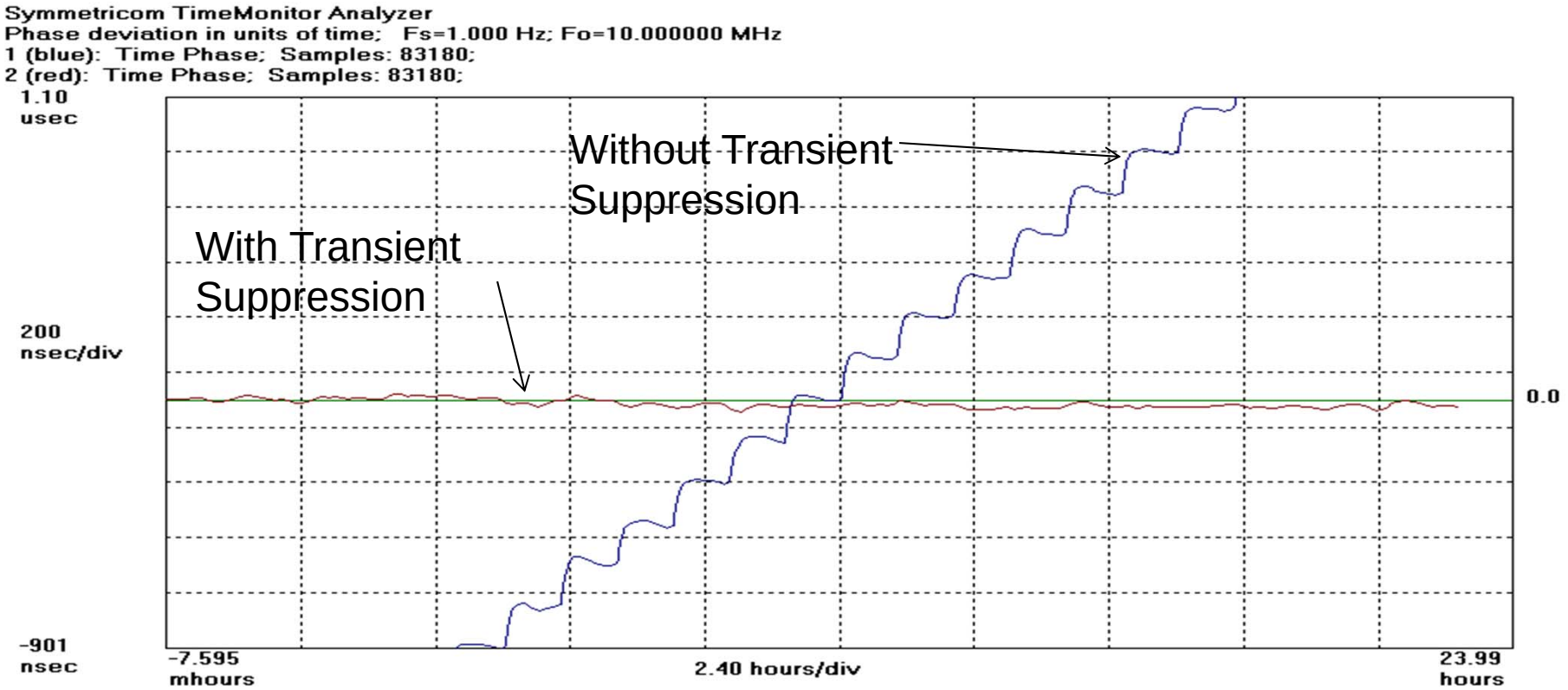
- 24 Hour Test: 8 hours PTP then 8 hour PTP outage then 8 hours PTP
- Soft Clock 2.1 Gateway Clock with **low cost** mini oTCXO
- 5 Node network for PTP transport based on real Metro Multi-Service Platforms stress with dynamic loading case TC12, TC13 and TC14.
- Time Error less than 175ns for all cases including 8 hour PTP outage



Synchronous Ethernet for Frequency Only Re-arrangement Transients

- 24 Hour Test: Synchronous Ethernet used as Frequency Input (No Time Input)
- Soft Clock Gateway Clock with **low cost** mini oTCXO
- A 150 ns re-arrangement (as permitted in G.8262) event occurs once per hour.



Synchronous Ethernet with PTP Independent Frequency and Time

- 24 Hour Test: Sync. Ethernet Frequency Input and PTP TC12 5 node for Time
- Soft Clock 2.1 Gateway Clock with **low cost** mini oTCXO
- Two SE frequency offset cases: Normal: 0.01 ppb and Holdover 0.1 ppb
- PTP Time output is identical unaffected by SE frequency offset.