Time synchronization with partial on-path support

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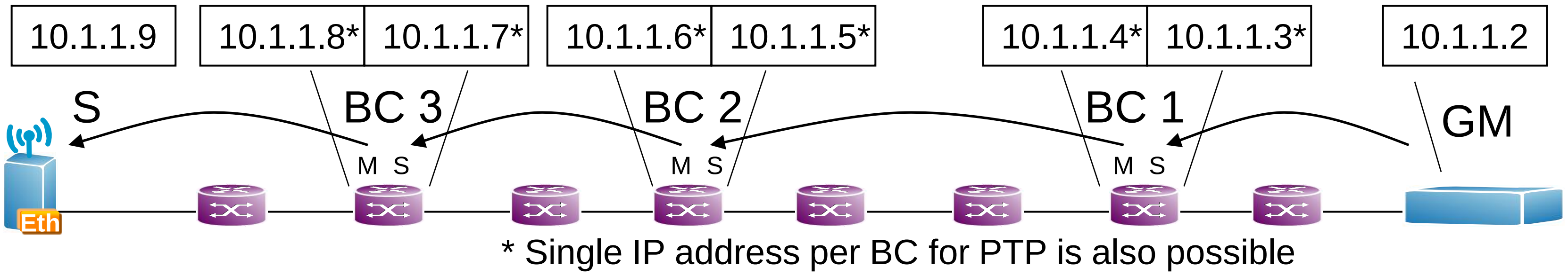
There are not yet common practices regarding partial on-path support techniques. The concepts in this presentation are lent partly from reviewed work presented by others. However, the presentation contains also initial thoughts that will probably evolve over time.

Partial on-path support profile

- The first contributions regarding the partial G.8275.2 profile have been addressed in ITU-T Q13/SG15.
- The profile might utilize ITU Telecom frequency profile G.8265.1 messages supplemented with time traceability information or IEEE-1588 default profile messages with IP unicast mapping, Annex A.9.
  - The default profile messages already include time traceability information.



S: slave, M:master, BC: boundary clock, GM: grandmaster

Classification

Full on-path support, ITU-T G.8275.1, planned to be approved in July.

- Single-link multicast Ethernet for ease of configuring
- All timing packets are utilized for synchronization.
- Packet rate 16 pps (packets per second)

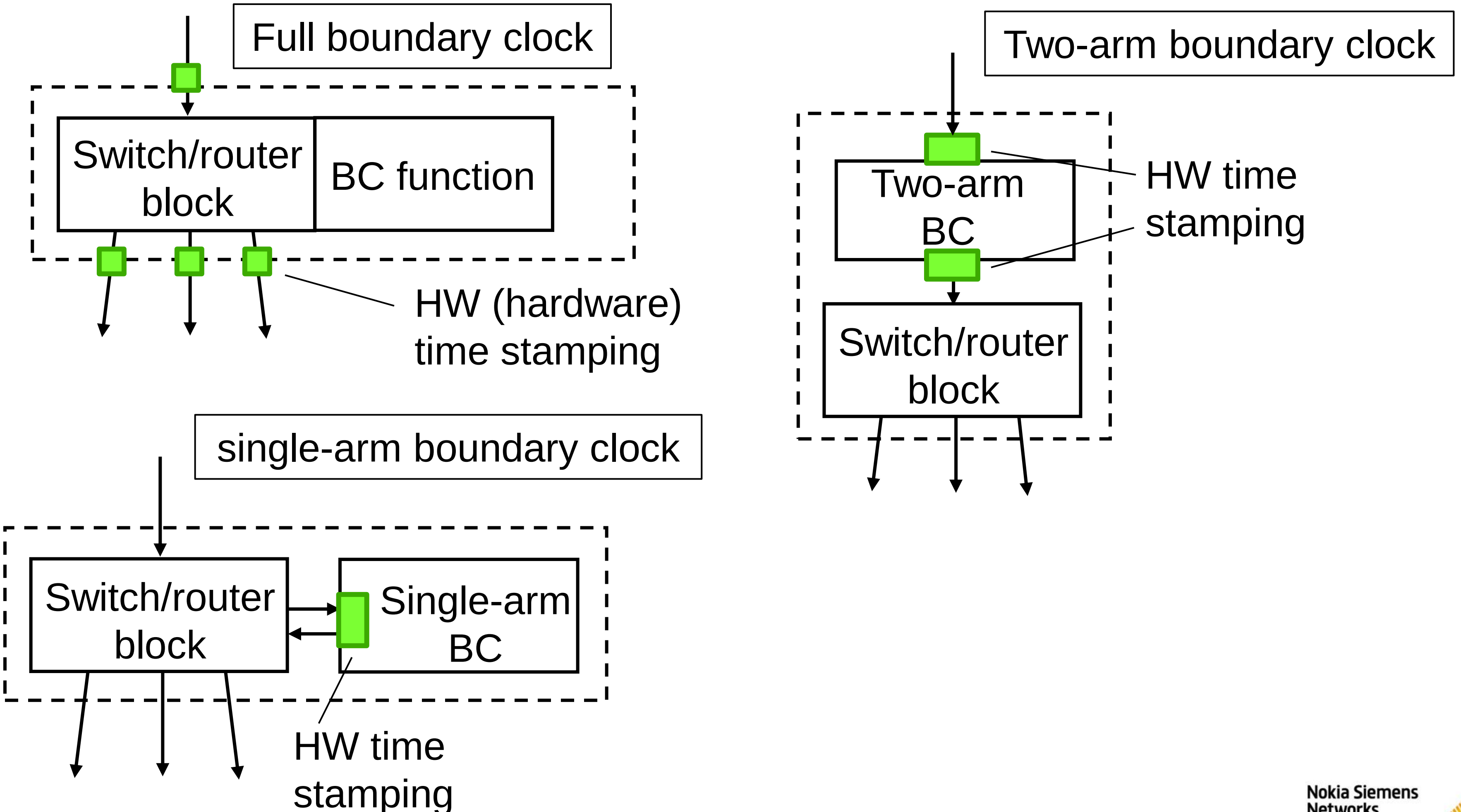
Partial on-path support ITU-T G.8275.2, no text incorporated yet into the draft.

- Unicast IP for allowing multi-hop paths between nodes supporting PTP.
- According to initial study by the author, only up to the fastest 1 % of packets should be utilized. Feasible for BCs and slaves but not for TCs*.
- Since the time constant of the PLL (phase locked loop) must be rather small, higher packet rate is preferred to allow efficient packet filtering and noise removal by averaging, for example 64 pps.

*TC: transparent clock

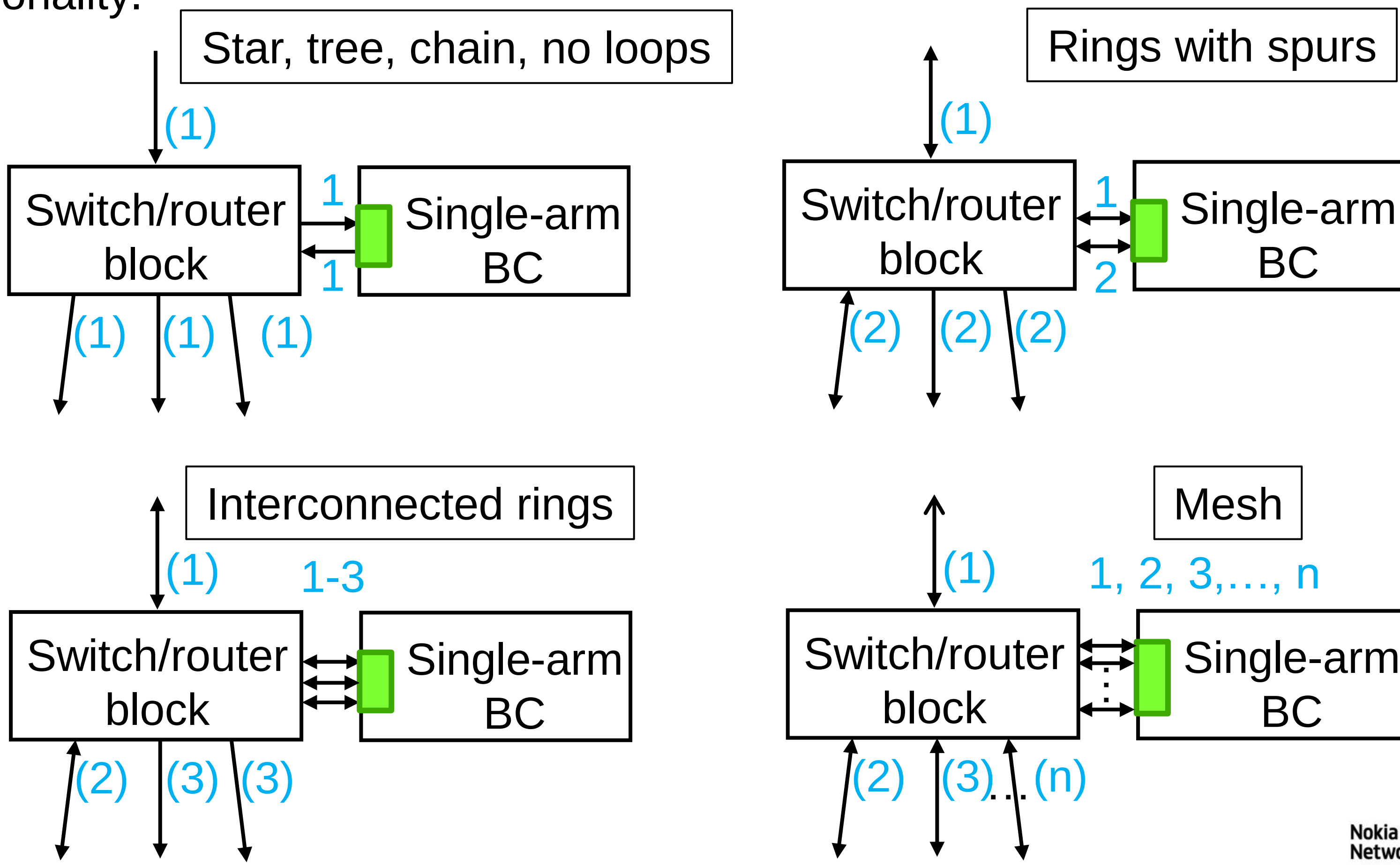
Implementation classes

- Although full boundary clock is the ultimate goal, intermediate solutions, single-arm and two-arm boundary clocks could be viable.
- At least single-arm clocks are already available.



Possible single-arm BC variants

- Single-arm clock could have one or more port identities.
- Ports of a BC that may be interconnected through a network loop may require separate port identities so that the Best master algorithm can function properly.
- The text boxes indicate, which type of topologies might take advantage of the functionality.

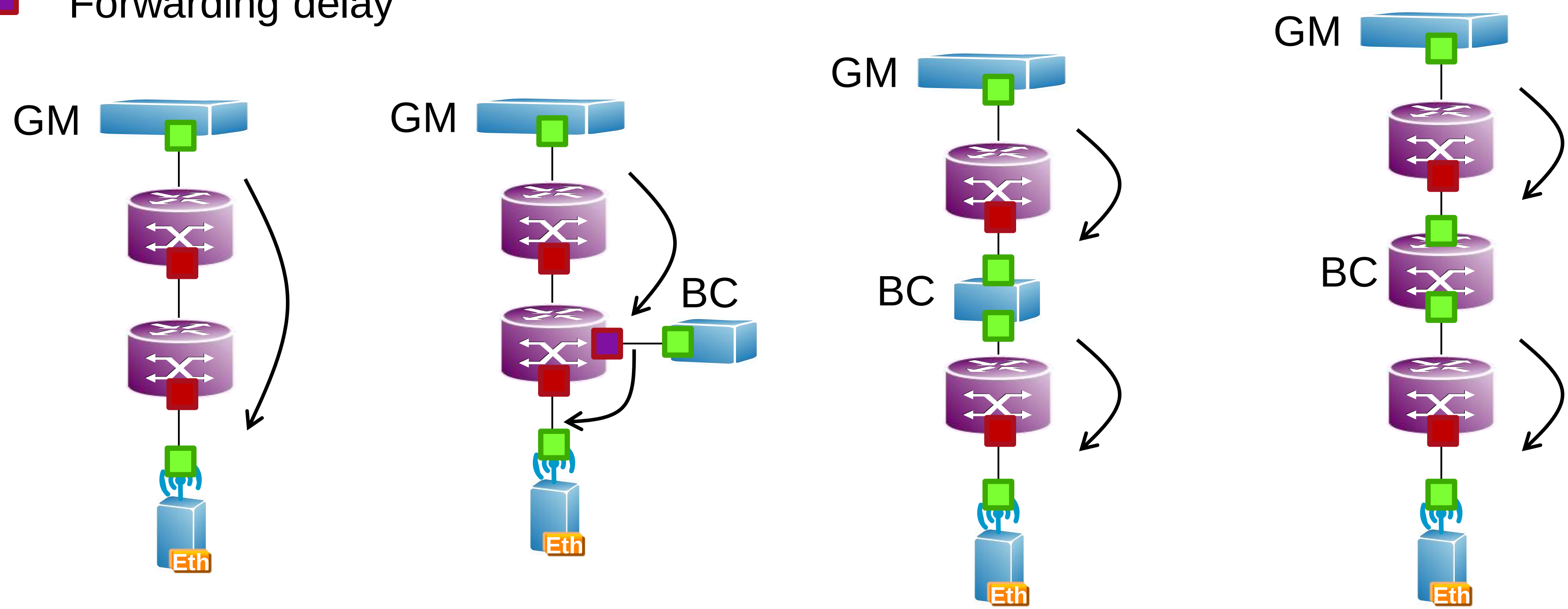


Counting PTP unaware hops – 1 x 2, 2 x 1, etc.

- External single- and two-arm BCs could time enable existing networks.
- Each full BC brings an additional hop for “free” compared to a single-arm or two-arm BC.

HW time stamping
Forwarding and queuing delay
Forwarding delay

Number of PTP hops — $N_P \times M_P$ — Number of PTP unaware nodes between BCs



1 x 2 un-aware hops

Single-arm BC

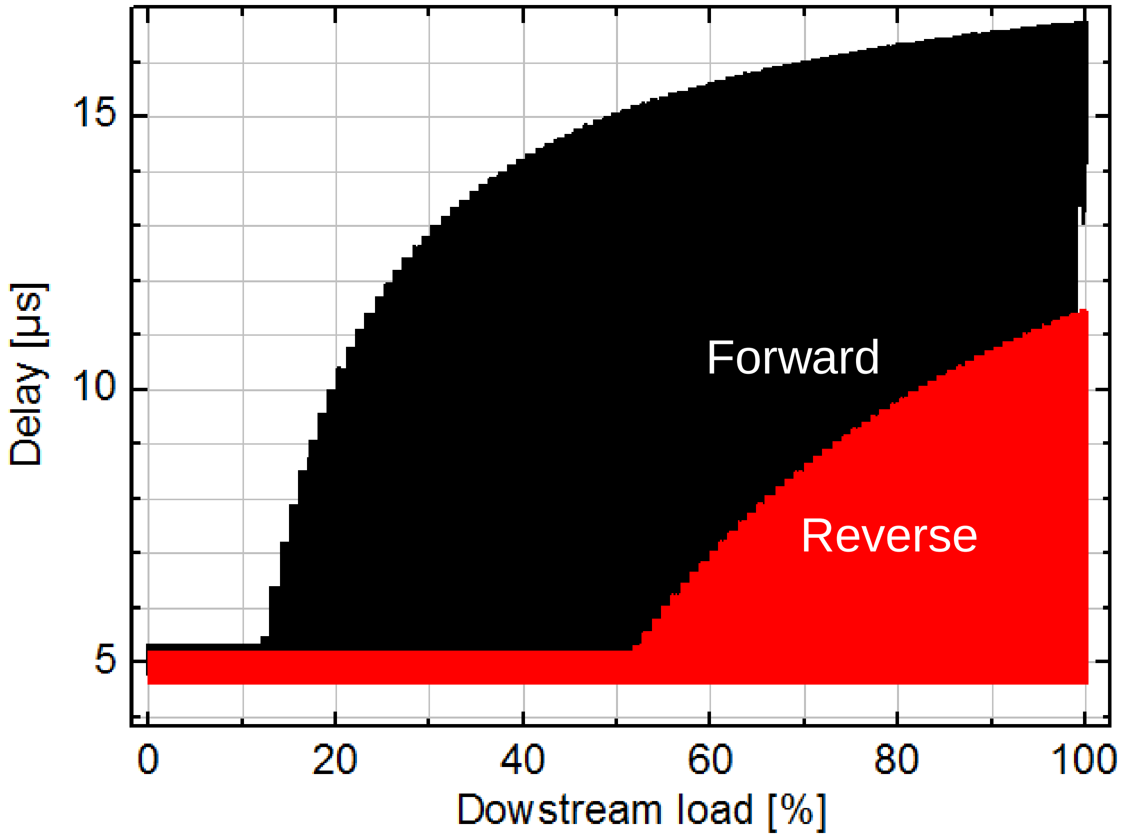
Two-arm BC

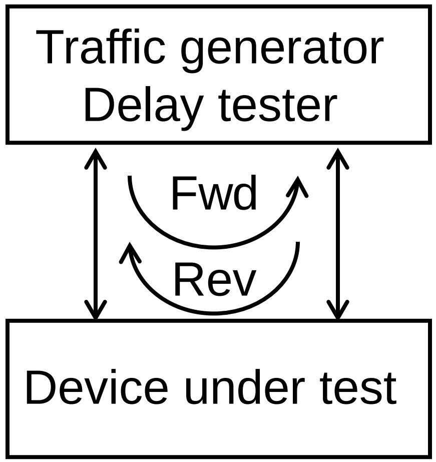
Full BC

2 x 1 unaware hops

Delay measurements, cell site switch

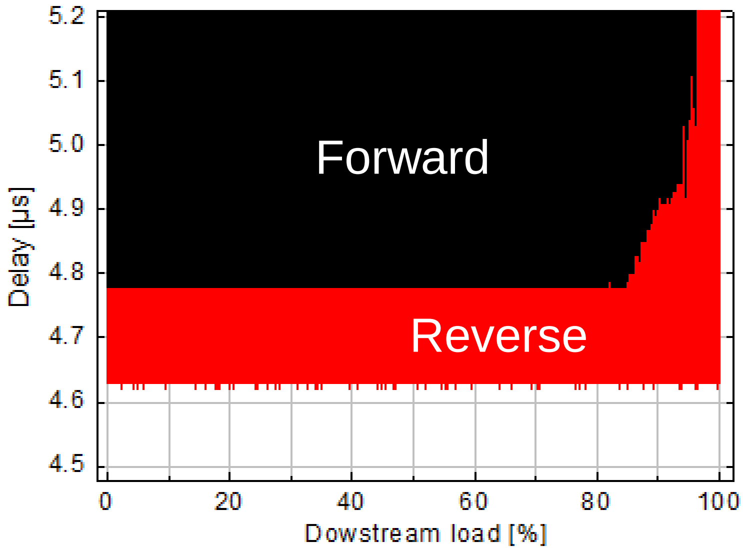
- Downstream load varies from 0…1 Gbit/s (port speed).
- For creating load based asymmetry, upstream is ¼ of the downstream load. The 4:1 load asymmetry has been used throughout the paper.

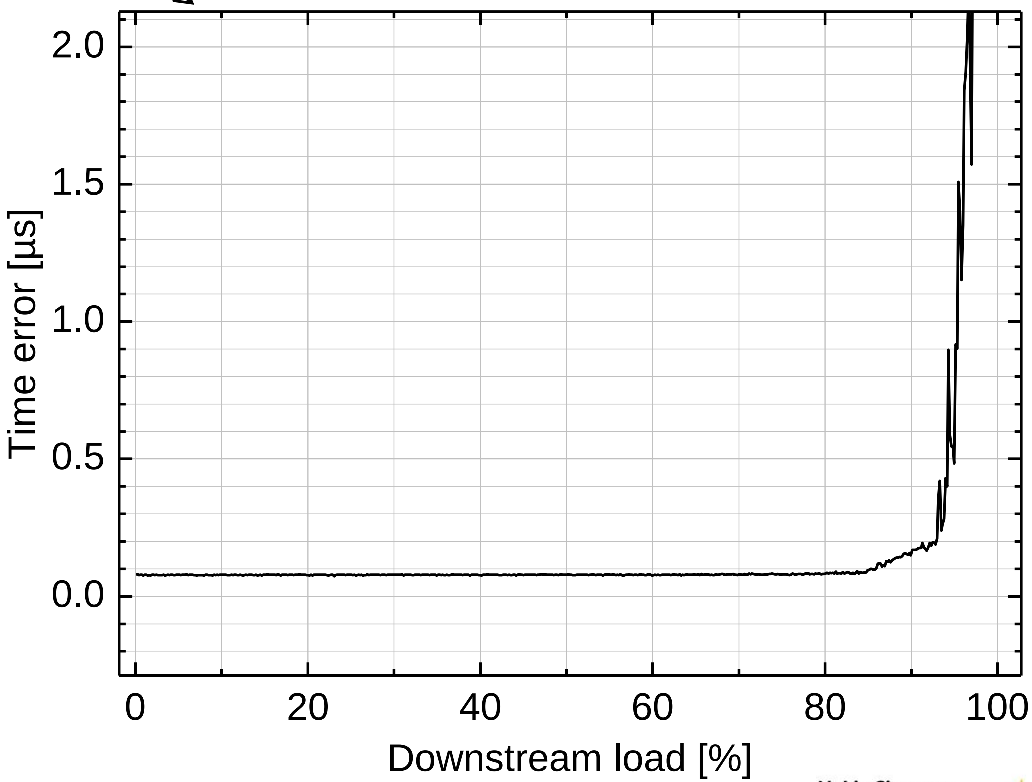




Error estimation from delays, single hop

- The 1-% shortest delays from each 2000-sample window are averaged to create a data set with a single value for each window, separately for forward and reverse. From the new dataset, calculate for each window:
- $error = \left(delay_{rev} - delay_{fwd}\right)/2.$



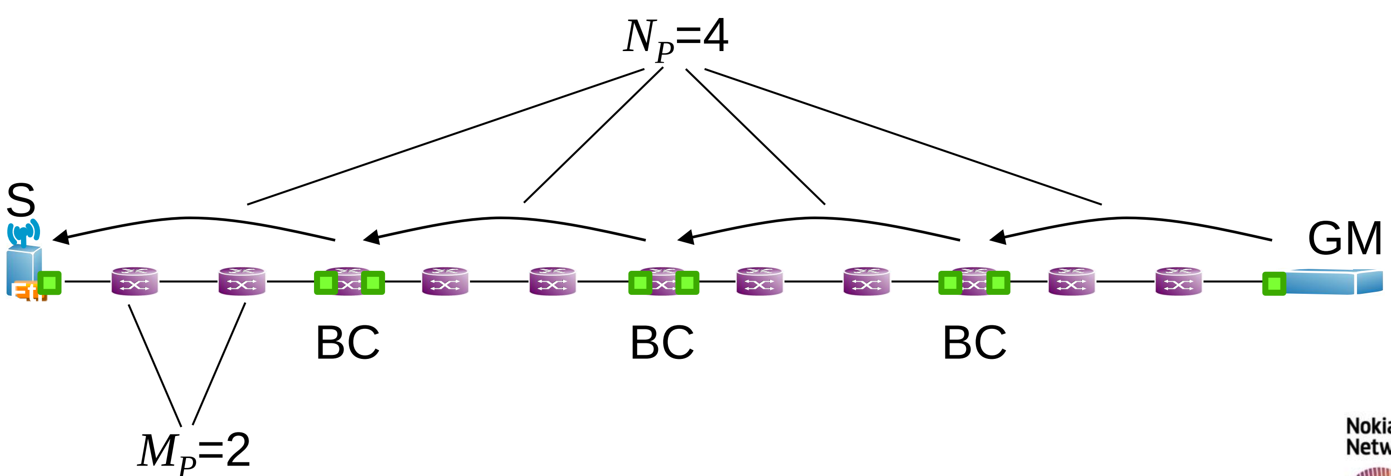


Error estimation for an N_P x M_P chain

- Add PTP unaware hops by adding the same delay to itself M_P-1 times while shifting the data 100 samples before each addition to remove short-term correlation.
- Average the fastest delays and calculate errors from the forward and reverse averages as explained in the previous slide.
- Add the error to itself N_P-1 times for estimating the error of the whole chain.

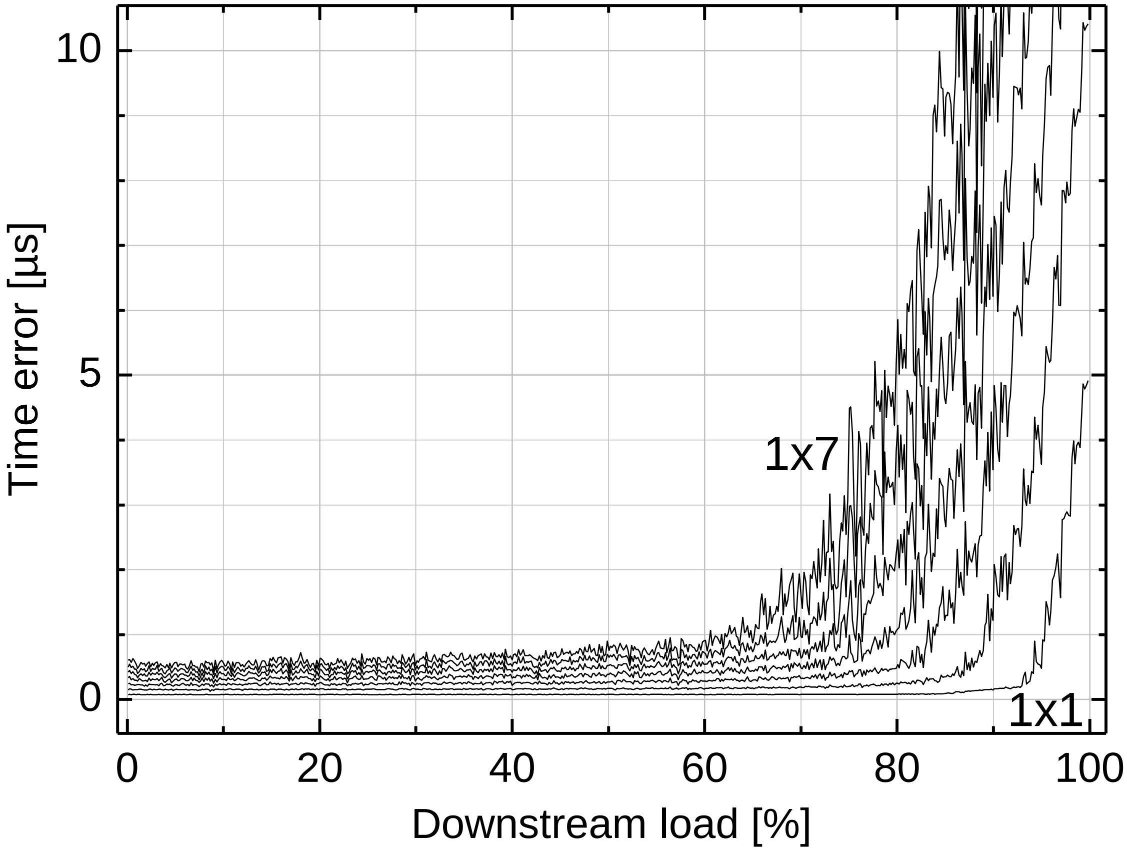
Total number of hops, full BC: $n_{full\_BC} = N_P \cdot M_P + N_P$

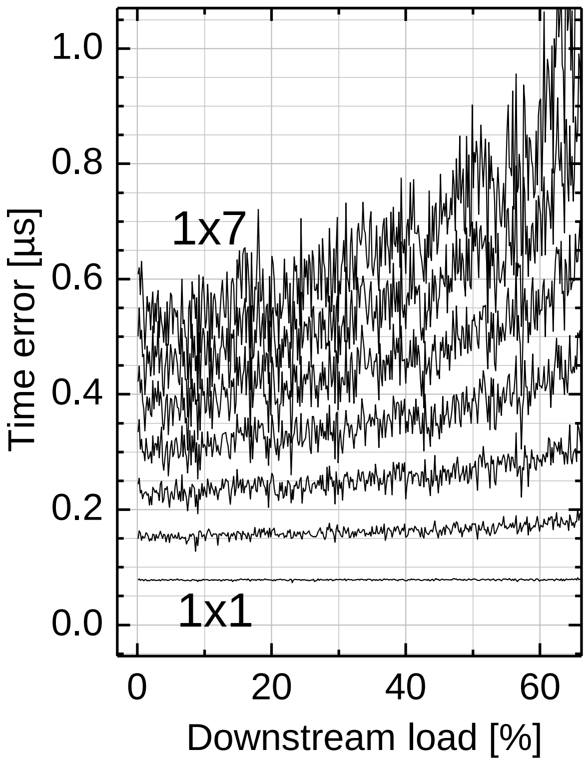
Single/two-arm BC: $n_{single\_arm\_BC} = N_P \cdot M_P + 1$



Time error estimate, cell site switch

- Hop counts from 1 to 7, i.e. 1x1-hop to 1x7-hop configurations, see p. 9.
- A load-independent asymmetry of 150-ns causes a 75-ns time error
- If the same error with same sign would be in all nodes, the error would add up linearly, see below.





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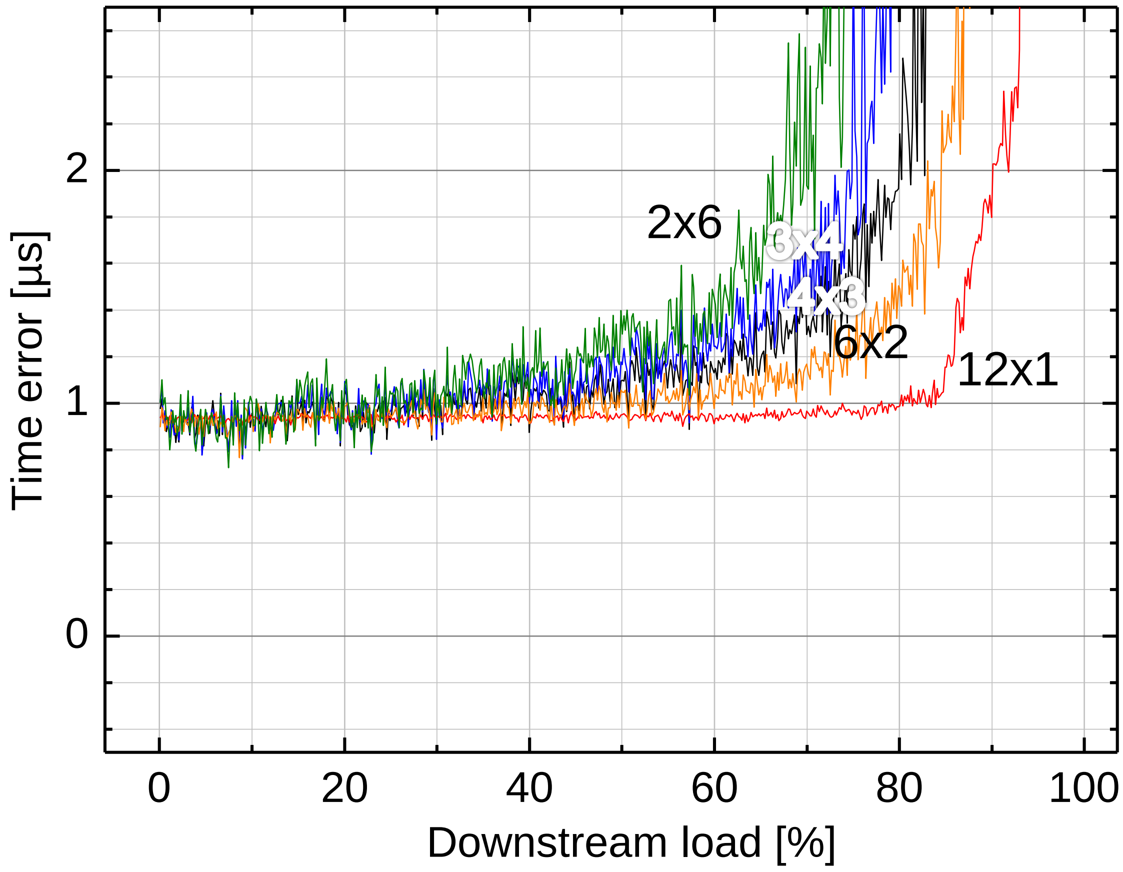
Cell site switch, N_P x M_P = 12, time error with different BC- vs. unaware-node configurations

- The fixed asymmetry cannot be filtered in BCs and could use the whole error budget ~1 µs if the sign of the error in each node has the same sign.
- In practice, the error can take either sign, usually canceling a large proportion of the error.



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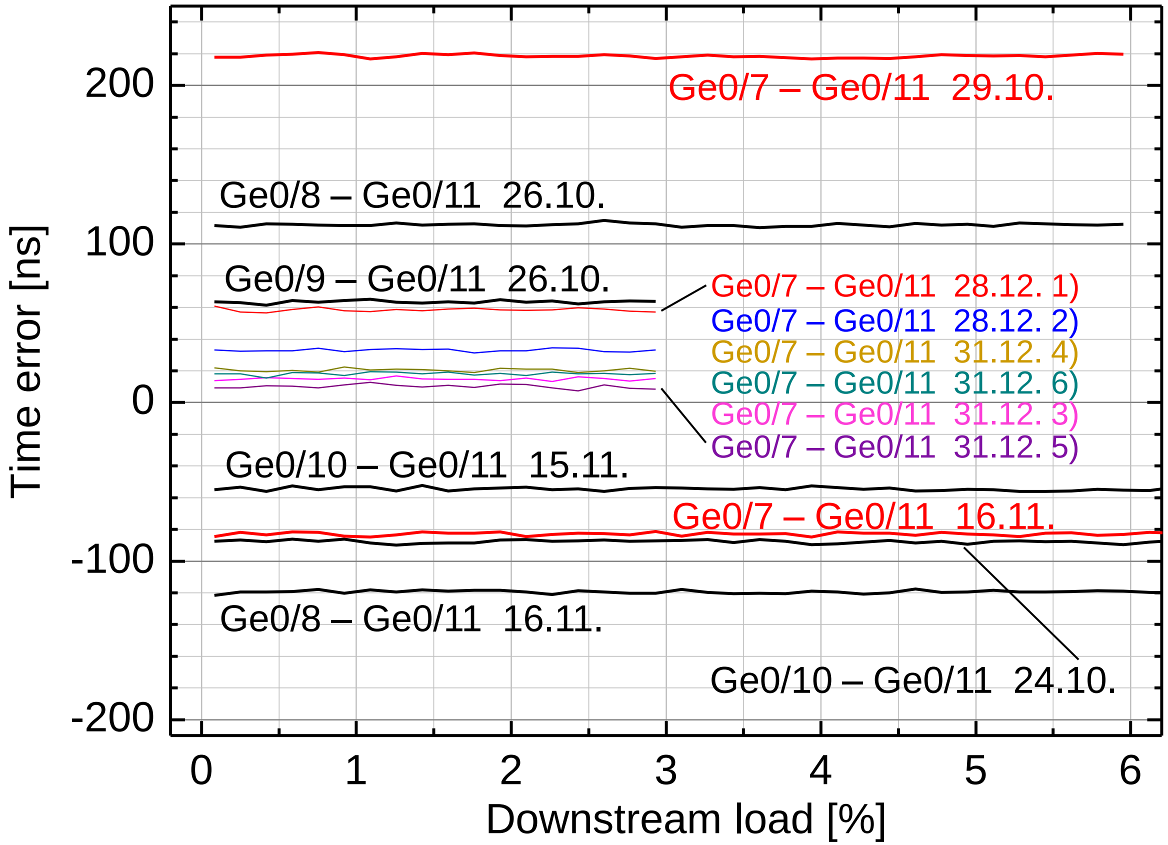
Consideration on how the fixed errors add up

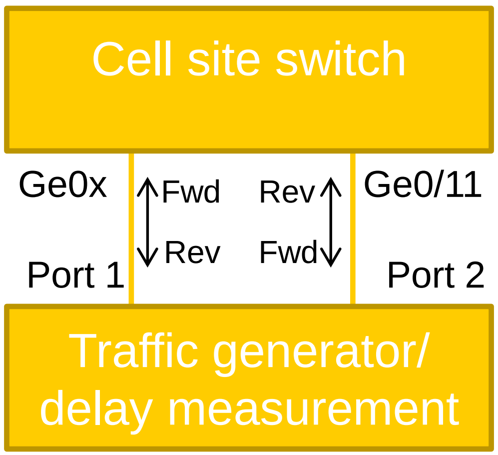
- The table below shows probabilities of the combined static error when adding up 12 times randomly plus- and minus-sign100-ns time errors.
- There is a small probability that the majority of error components on a path take the same sign. In this case, the fixed asymmetry consumes a large proportion of the total budget. However assuming 100-ns error in every interface is a somewhat pessimistic assumption.

0.0 µs	≤ 0.2 µs	≤ 0.4 µs	≤ 0.6 µs	≤ 0.8 µs	≤ 1 µs	1.2 µs
22.6 %	61.2 %	85.4 %	96.1 %	99.4 %	99.95	0.05 %

Cell site switch fixed asymmetry – fiber interfaces

- Different port combinations produce different time errors. Also the same port combination gives different results, see the 8 measurements of Ge0/7 – Ge0/11.
- Surprisingly, in the last measurement sequence all results are within 50 ns even though the equipment was reload booted between 1), 2), and 3), and power-cycled between 3), 4), 5), and 6).





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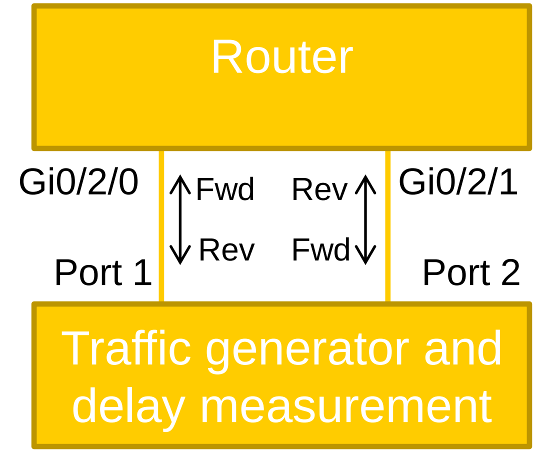
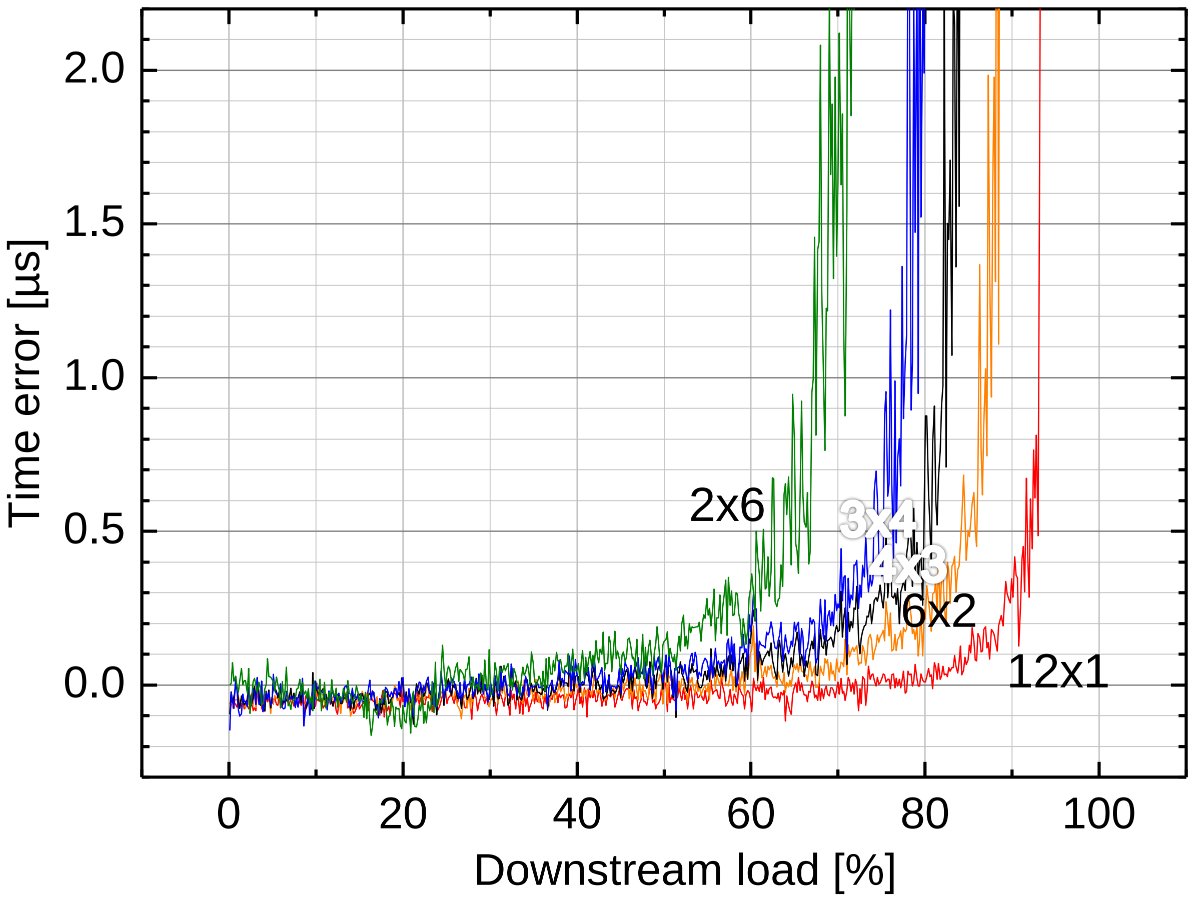
Aggregation router

- The fixed asymmetry of this port combination is very small.





Configuration	Load at 1-µs error
12 x 1 hops	93 %
6 x 2 hops	86 %
4 x 3 hops	82 %
3 x 4 hops	77 %
2 x 6 hops	67 %

Networks

Fixed asymmetry error measurements

- Most equipment were measured only once. The exceptions are marked.

Equipment	Error caused by asymmetry
Cell site switch[1]	-120…+220 ns
Aggregation router[2]	0…70 ns
Cell site router	95 ns
Aggregation switch	< 10 ns
Aggregation and edge switch	35 ns
FDD microwave radio	< 5 ns
FDD microwave radio[3]	500 ns, 50 ns, 60 ns, 110 ns
TDD microwave radio	50 ns

[1] 14 independent measurements
[2] 3 independent measurements
[3] One measurement for 14 MHz QPSK, 256QAM, 28 MHz 64QAM, and 56 MHz 32QAM, respectively

Conclusions

- Partial on-path support seems to be feasible if it is possible to limit the traffic to 70-90 % of bandwidth depending on BC configuration.
- A network with 4x3 Gbit/s links could be operated at 80-% load in all nodes if the fixed asymmetry build-up is limited to 0.5 µs.
- Bursts reaching 100 % and lasting few seconds at a time could be still allowed.

For further study

- The partial on-path support community should study different network scenarios to understand, which functionalities in the PTP clocks are required for reliable operation and which are not.
- The protocol behavior of the master and slave remains probably similar to the behavior in the frequency profiles.
- Regarding boundary clocks, topologies to consider: 1) Tree structures commonly used for the final 2-4 hops in cellular networks 2) Access rings with spurs 3) Interconnected rings 4) Mesh.

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