MICROPROCESSOR-BASED SATELLITE-CONTROLLED CLOCK

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Abstract

As a demonstration of the usefulness of the NBS-sponsored time signals from two U.S. weather satellites, NBS designed and built a "Satellite-Controlled Clock." The initial design used random logic requiring nearly 80 packages of TTL logic. With the advent of microprocessors, the clock was redesigned using a four bit microprocessor and a scientific calculator chip.

Today, commerical versions of the NBS-designed clock are available and are finding use in the electric power industry, radio and television broadcasting, defense, communications, and geophysical monitoring.

The evolution of the satellite-controlled clock from random logic to commercial products using eight bit microprocessors are discussed in some detail.

Introduction

In May 1974, the Time and Frequency Division of the National Bureau of Standards (NBS) added a time code to a continuous data stream transmitted from the National Oceanic and Atmospheric Administration's (NOAA's) Geostationary Operational Environmental Satellite (GOES) satellites. The time code not only contained the usual information of days, hours, minutes, seconds and a UT1 (astronomical time scale) correction but added new information. That information was included to provide the user the capability of computing the propagation delays between the master clock and his location via the satellite. That information was the transmitting satellite's current position in terms of it's subsatellite longitude, latitude, and height above the surface of the earth.

The combination of a satellite-disseminated time code and an easily computed propagation delay had all the elements of a greatly advanced system for time distribution. To demonstrate the capabilities of this advanced timing system and to accelerate and encourage the transfer of its technology to users and industry, NBS developed the instrumentation, a decoder clock, to recognize the time code, set, and control ground based clocks. This instrumentation was first embodied in mid 1974 as random logic circuitry. The advent of microprocessors led NBS in 1975 to replace the random logic design with a 4004* microprocessor yielding an improved instrument which was completely automatic.

Today, this work has fostered the development of similar commercial instruments using 8080 and 6800 microprocessors. These instruments are now being used in the electric power industry, defense, geophysics, communications and the broadcast industry.

The evolution of the satellite-controlled clock is discussed in this paper and adds to the growing list of illustrations of microprocessors simplifying what was once a complicated if not impossible instrumentation problem.

Details including schematics, board layouts, flowcharts, and software of the actual NBS designed instruments have been completely documented in the references and therefore will not be discussed in this paper.

Definition of the Instrumentation Problem

Available from a receiver (the receiver is not part of the instrumentation development to be described here) are two outputs--data and data clock. The data consists of binary "0's" and "1's" each 10 ms in duration. The data clock is a 100 Hz square wave with its negative going transitions simultaneous with the mid point of data bits (see figure 1).

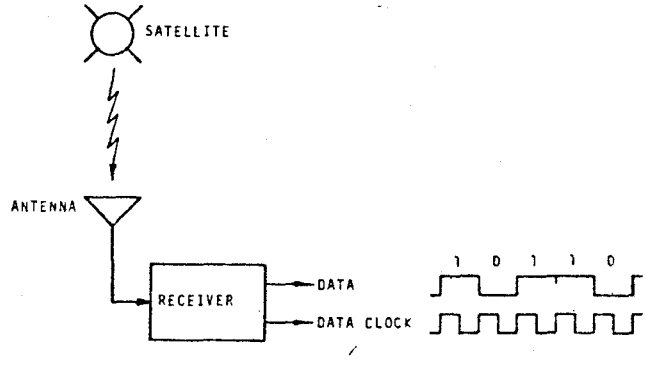

FIGURE 1. INPUTS TO THE DECODER-CLOCK

*The use of trade names is necessary to specify the components; it does not imply endorsement by NBS.

The data stream contains the time code which is time division multiplexed with other data. The data stream consists of repeated sequences of frames of four bits representing a binary coded decimal (BCD) word of the time code beginning on the one-half second followed by a maximum length sequence (MLS) 15 bits in length used for message synchronization and ending with 31 bits of data not related to the time code or frame synchronization (see figure 2).

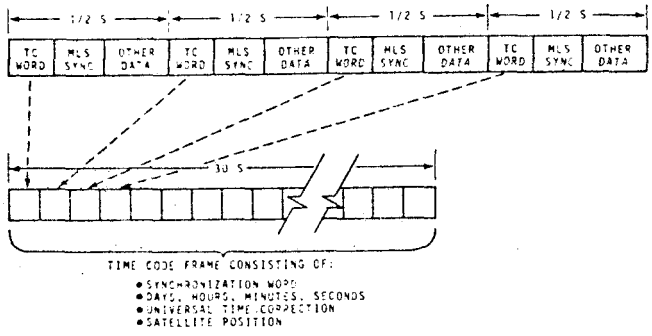

FIGURE 2. GOES DATA STREAM

The data rate is 100 b/s and is determined by atomic oscillators. Each message frame is one-half second in length (50 bits). The time-code frame, made up by gathering together four bits from each frame begins on the half minute as shown in figure 3.

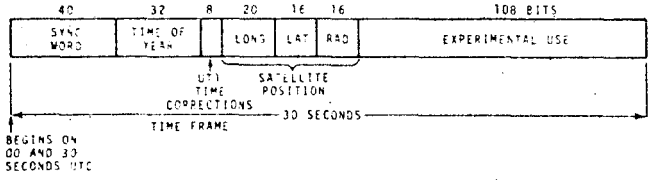

FIGURE 3. TIME-CODE FORMAT

The time-code frame contains its own synchronization word, a time-of-year word, UT1 correction, and the satellite's position.

A decoder clock, to be effective, must perform, as a minimum, the following functions:

1. Detect the negative going transitions of the data clock and immediately sample the data to determine if it is a binary "0" or "1".

2. Search 15 consecutive bits of data for the MLS synchronization pattern (100010011010111).

3. From the end of the frame sync word, "count" 31 bits to the beginning of a time-code word, extract four bits, and store.

4. Examine ten consecutive time-code words for the time-code synchronization word and detect its occurrence.

5. Set the internal "date clock" with the received time-of-year word, the location of which was found in step 4. above.

6. "Store" UT1 and satellite position data.

7. Update the date clock by counting data-clock transitions; each count incrementing the date clock by 10 ms.

8. Compare the date clock with subsequent time-of-year messages received from the satellite.

9. Display decoded data and the time of year.

10. Output a 1 pps electrical pulse and a standard time code such as IRIG-B.

Instrumentation

Random Logic Solution

The above ten functions were first realized in 1974 using entirely transistor transistor logic (TTL) random logic. Figure 4 shows the instrument which contained nearly 80 integrated circuit packages. The unit presented significant cost, power consumption, and reliability problems that were undesirable and prompted NBS to look for simpler solutions.

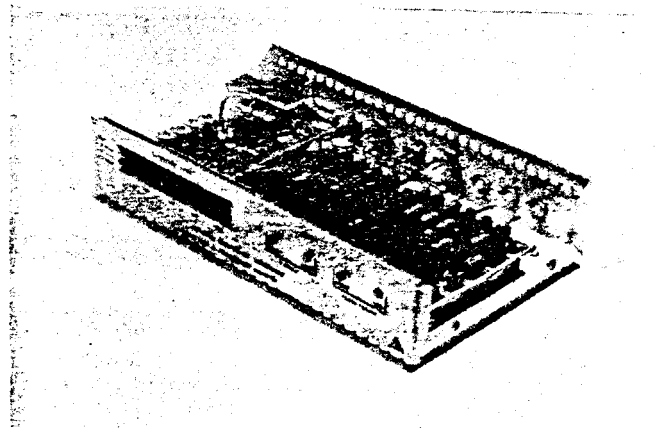

FIGURE 4. RANDOM LOGIC DECODER CLOCK

This decoder clock also had no computational capabilities. NBS compensated for this deficiency by designing a plastic slide rule to compute the propagation delays. The slide rule, shown in figure 5, computed the free-space distance, r, in microseconds between the ground and satellite. The distance, r, in microseconds is given by

$$r = \frac{\sqrt{R^2 + h^2 - 2Rh\cos\beta}}{C},$$

where C = 0.2997925 km/μs,

$$h = a \sqrt{\frac{1 + \frac{b^4}{a^4} \tan^2 \phi}{1 + \frac{b^2}{a^2} \tan^2 \phi}},$$

$$\cos \beta = \sin \phi_r \sin \phi_s + \cos \phi'_r \cos \phi_s \cos |\lambda_s - \lambda_r|,$$

$$\tan \phi' = \frac{b^2}{a^2} \tan \phi,$$

r is the distance from the earth's center to the satellite,

ϕ' is geocentric latitude,

ϕ is geodetic latitude,

b is the earth's semiminor axis (6356.5838 km),

a is the earth's semimajor axis (6378.2064 km),

and the subscripts r and s refer to the earth's surface and satellite respectively.

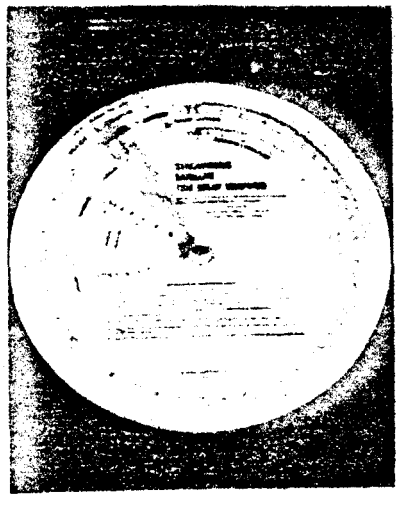

FIGURE 5. PROPAGATION DELAY SLIDE RULE

Four-bit Microprocessor Solution

It was fortuituous that microprocessors were becomming available when NBS began looking for a means of simplifying and improving the random-logic based decoder clock. NBS accomplished a new instrument design using a 4004 microprocessor and integrating it with a scientific calculator chip to perform the path delay calculations discussed previously. This microprocessor-based instrument is shown in figure 6. The unit, in addition to the ten basic functions mentioned, computed delays between the master clock and its location on the earth's surface via the satellite. The block diagram in figure 7 illustrates the functions. Thumb wheel switches input the user's longitude and latitude. The microprocessor and calculator chip computes delays and compensates for them by controlling a programmable delay generator so the 1 pps output is in synchronism with the NBS master clock Coordinated Universal Time (UTC)NBS.

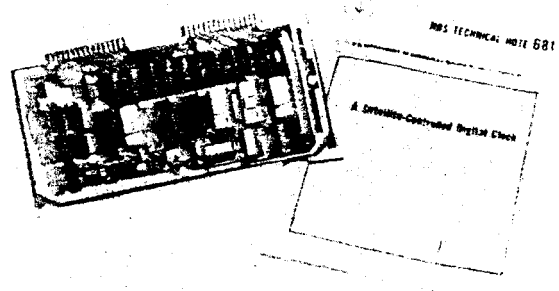

FIGURE 6. SATELLITE-CONTROLLED CLOCK USING THE 4004 MICROPROCESSOR

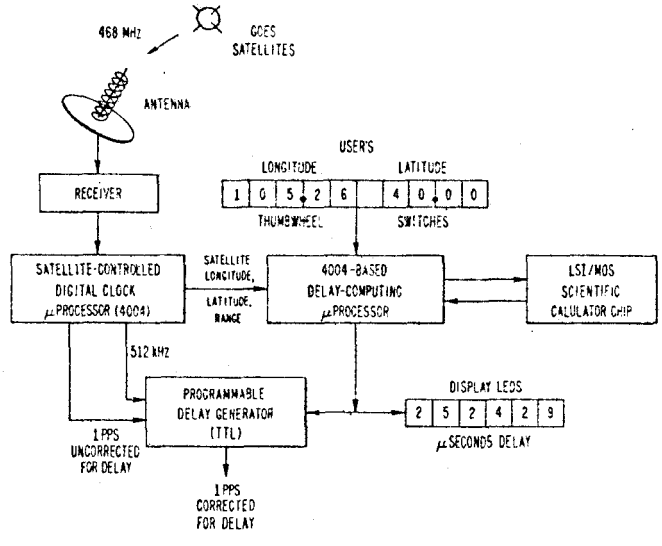

FIGURE 7. BLOCK DIAGRAM OF 4004 DECODER CLOCK

Commercial Clocks

The basic approach to the satellite-controlled clock taken by NBS has recently led to two commercial versions of the instrument. One unit is the "smart" clock shown in figure 8 and uses a 8080 microprocessor. It sells for a little over $4000 including a

receiver and antenna. Another version uses a 6800 microprocessor to obtain all functions except automatic path delay corrections. This clock and receiver, shown in figure 9, sells for approximately $2000 depending upon options.

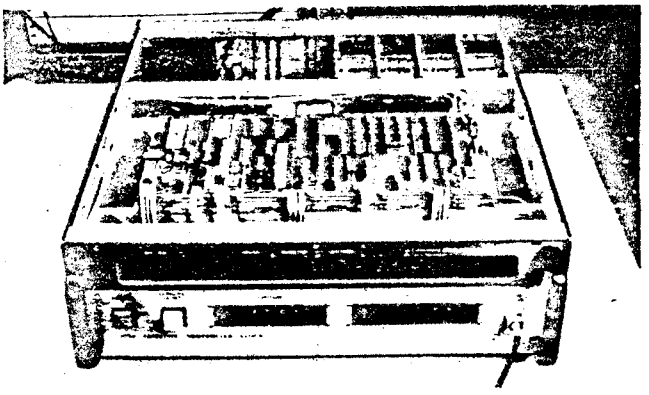

FIGURE 8. COMMERCIAL "SMART" CLOCK USING AN 8080

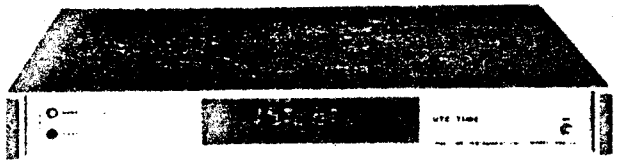

FIGURE 9. COMMERCIAL CLOCK USING AN 6800

NBS has been contacted by more than 18 manufacturers interested in developing products of a similar nature.

Conclusions

The capability of the microprocessor to simplify and add capabilities to the satellite-controlled clock was shown. The satellite-controlled clock, by virtue of using satellite-transmitted signals and being completely automatic by use of microprocessors, has made the GOES time dissemination system the most viable and exciting new source for synchronization today. This is particularly true for users with more than casual interests. Presently, the GOES time system is being considered for use with European and Japanese satellites. A major reason for its acceptance by other countries has been its automatic recovery features made possible by microprocessors.

References

1. Cateora, J. V., Davis, D. D. and Hanson, D. W., "A Satellite-Controlled Digital Clock," NBS Technical Note 681 (June 1976).

2. Hamilton, W. F. and Hanson, D. W., "A Synchronous Satellite Time Delay Computer," NBS Technical Note 638 (July 1973).

3. Cateora, J. V., Hanson, D. W. and Davis, D. D., "Automatic Path Delay Corrections to GOES Satellite Time Broadcasts," NBS Technical Note 1003 (to be published April 1978).