# RF Local Oscillators for Low-Power Chip-Scale Atomic Clocks

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**ABSTRACT** | Accurate timing is critical in many industries, from time-stamping grocery receipts to facilitating stock-market transactions and supporting precise navigation, localization, and guidance. High levels of precision are currently achieved using physically large, power-hungry atomic clocks that rely on energy-level transitions in a chosen atomic species. Recently, commercially available chip-scale atomic clocks (CSACs) have emerged, offering atomically precise timing in a compact, low-power package that can be operated on a battery for extended periods. Such clocks have important applications in underwater timing for oil and gas exploration, enhanced GPS receivers, and are being adopted for application to the energy grid, where large clocks are impractical. These devices contain a microwave local oscillator (LO) that generates the RF used to interrogate the atoms and, once locked to the atomic resonance, serves as the clock output. This article reviews the state of the art in microwave CSACs, with a focus on the engineering requirements for compact, low-power microwave LOs used to lock to the atomic transition. Several different LO designs are surveyed and compared in terms of power consumption, phase noise, and suitability for use in miniaturized clocks. The frequency control electronics needed to operate CSACs are also discussed. Finally, potential future improvements to all clock electronics for CSACs are highlighted.

**KEYWORDS** | Clocks; microwave circuits; microwave oscillators; oscillators; phase noise.

## I. INTRODUCTION

Time keeping plays a critical role in many high-volume applications, e.g., navigation and stock-market business transactions. In the field of metrology, time and frequency standards provide the most precisely measurable unit, the second, which subsequently underpins other dimensional metrology units, such as the meter, kilogram, and ampere. The high level of precision required for metrology and other applications is currently obtained using large and power-hungry atomic clocks, which use electromagnetic waves at optical or microwave resonance frequencies to cause energy-level transitions in an atomic species. This accurately kept time is then often distributed via GPS, the Internet, and radio to various platforms around the world. In the last 20 years, miniaturized low-power atomic clocks referred to as chip-scale atomic clocks (CSACs) using microwave atomic transition frequencies have been a topic of research and development, becoming especially important in GPS-denied environments such as the deep ocean and space, where they are currently in use. A simplified CSAC is illustrated in Fig. 1(a), showing the microwave local oscillator (LO), control circuits, quartz crystal, glass vapor cell containing alkali atoms (Cs or Rb), photodetector, and semiconductor laser, mounted on

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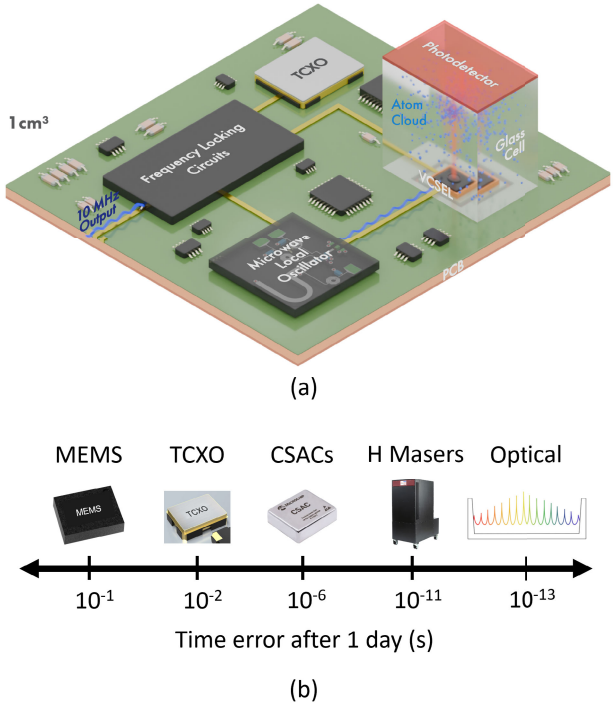


**Fig. 1.** *(a) Simplified illustration of a vapor cell CSAC based on a CPT interrogation scheme. This architecture is the most prevalent in commercialized CSACs. (b) Time error after one day in (s), representative for MEMS, TCXO, CSACs, hydrogen masers, and optical clocks based on [1] and [2].*

a printed circuit board (PCB). This clock provides an atomically defined 10-MHz output.

Atomic clocks [3], [4], [5] are based on transitions in atoms whose frequencies depend largely on the laws of quantum mechanics and fundamental constants of nature such as the fine structure constant and the Bohr magneton. As a result, unlike classical resonators, every isolated atom of a given species has exactly the same transition frequency, leading to excellent reproducibility in the output from clock to clock. In addition, the weak dependence of the clock frequency on external perturbations implies good long-term frequency stability and high accuracy, compared to, for example, mechanical resonators like quartz crystals. There are several types of atomic clocks: large-scale fountain, optical lattice, and optical ion clocks, among others. These achieve timing errors equivalent to 1 ns over many decades but are large, consume high amounts of power, and are difficult to build and operate. More compact clocks achieve correspondingly worse precision (1 ns–1 $\mu$s over one day) but are less expensive and more reliable, and have a size, weight, and power suitable for deployment in a far greater range of application spaces. Fig. 1(b) illustrates a stability comparison between different types of atomic clocks, which realize the second, underlie satellite-based navigation systems such as Global Navigation Satellite System (GNSS) [6], provide a backbone for secure communication [7], and can be used for deep-space navigation [8], [9]. The most common of these clocks is based on microwave transitions in alkali atoms, with transition frequencies in the gigahertz (GHz) range.

Passive atomic clocks, a subcategory of atomic frequency standards that includes CSACs, operate using an LO that interacts with an ensemble of atoms. The atoms act as a high-$Q$ frequency discriminator, generating an output signal that varies with LO frequency near the atomic resonance, as shown in Fig. 2(a). This signal is then fed back to the LO in a control loop, locking its frequency to the atomic transition and thereby imparting the atoms' stability onto the LO.

## A. Background

The properties of the LO play an important role in determining the clock performance. Often, the short-term (<1 s) fractional frequency stability of the microwave LO is considerably better than that of the atoms and, as a result, can determine the short-term stability of the clock as a

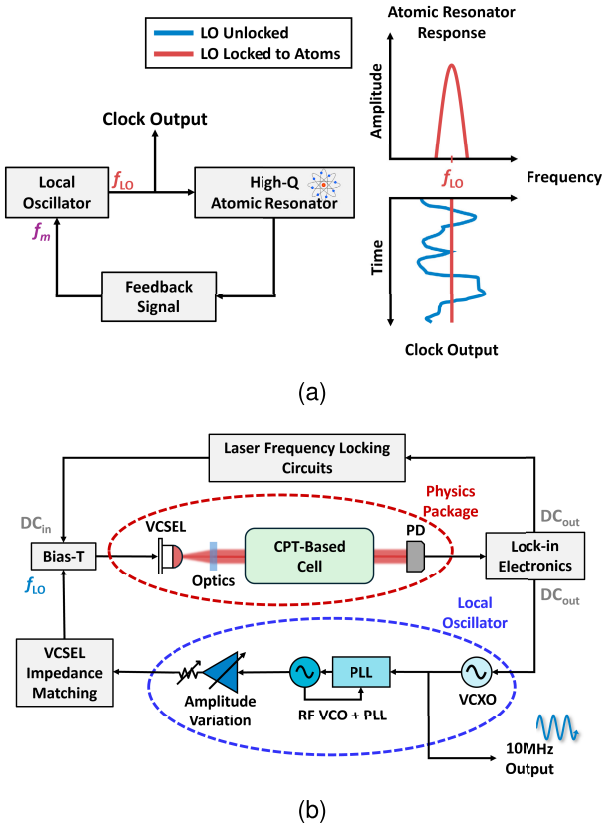


**Fig. 2.** *(a) High-level microwave atomic clock block diagram showing the process of locking to a high-$Q$ atomic resonator. On the right-hand side is an example of an atomic resonator response as well as oscillator frequency disciplined by the atoms. (b) Block diagram of a generic CSAC based on CPT, highlighting different parts of the microwave-frequency synthesis chain. Here, the "physics package" is defined as circled in red, while the microwave LO is circled in blue. Remaining abbreviations are explained in the main text.*

whole, as well as the time window for locking the LO to the atomic transition. Other properties of the LO such as the frequency drift and noise can also affect the stability of the clock, for example, by intermodulation and aliasing effects [10]. There are many types of microwave atomic clock designs, and each has its own set of LO requirements. High-performance atomic clocks require correspondingly high-performance LOs, while more compact, lower power atomic clocks require LOs that balance performance with additional size, weight, power, and cost (SWAP-C) requirements. In the past 20 years, a new generation of low-power atomic clocks has been developed [2], [11], [12], [13] based on the optical interrogation of alkali vapor cells in micromachined vapor cells without the need for bulky microwave cavities. Typical atomic species used in these microwave clocks are $^{133}$Cs and $^{87}$Rb due to their high vapor pressure, large hyperfine splitting, and simple electronic energy-level structure. These types of CSACs have been successfully commercialized [14] and are currently making an impact across a range of application spaces from underwater seismology [14] to space [15]. They typically require under 200 mW of DC power to operate and have a total volume on the order of 20 cm$^3$.

Fig. 2(b) shows a more detailed block diagram of an example CSAC based on a coherent population trapping (CPT) atomic interrogation scheme [16], [17], which is the dominant type of commercially available chip-scale clocks [1], [2]. For CPT-based schemes, instead of exciting the hyperfine transition in the atoms directly using a microwave field as is done in a traditional cesium beam clock, a pair of optical fields separated in frequency by the hyperfine splitting illuminates the atoms. Hyperfine coherences are generated through the nonlinear response of the atom to this pair of optical fields. Exciting the atoms using CPT-based methods has an advantage over traditional microwave clocks by removing the need for bulky microwave resonators, which are usually at least one-half of the wavelength of the microwave signal, on the order of 3 cm for $^{133}$Cs. Instead, CPT interrogation can rely on modulating the injection current of a vertical cavity surface emitting laser (VCSEL) diode [18], [19] to create sidebands on the emitted optical signal at spacings equal to the full ground-state hyperfine transition frequency (9.192 GHz for $^{133}$Cs), or subharmonics of that transition (4.596 GHz for $^{133}$Cs) [20]. These VCSELs can be fabricated in GaAs-based semiconductors at wafer scale, and, for example, can emit $\sim$1 mW of narrow linewidth light at 852 nm for the $^{133}$Cs D2 optical transition, while only occupying a few 100 $\mu$m$^2$ in individual size [2], [18], [19], [21], [22]. The components related to CPT such as the VCSEL, optics, and atomic sources are usually grouped together in what is referred to as a "physics package," as shown in Fig. 2(b), along with a small photo detector (PD) [23]. The components related to RF synthesis required for modulation of the VCSEL, such as microwave-frequency voltage-controlled oscillator (VCO), phase-locked loop (PLL), voltage-controlled quartz crystal oscillator (VCXO), and amplitude control circuits, are grouped together and defined here as parts of the microwave LO.

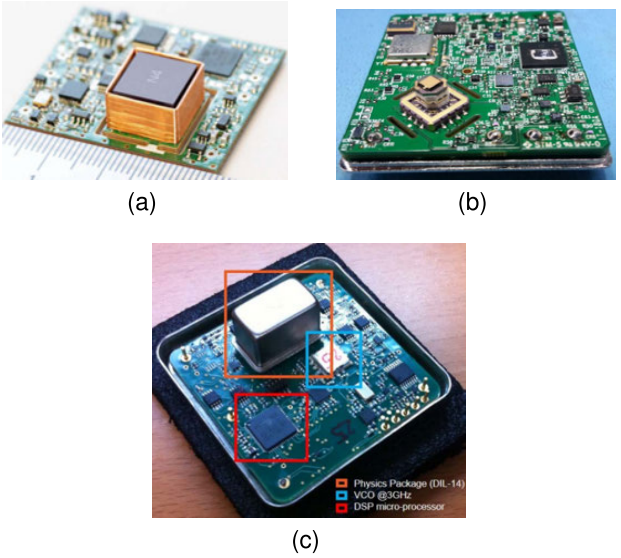


**Fig. 3.** *(a) Photograph of the "ULPAC: ultralow-power atomic clock," a Cs CPT-based clock using an LO integrated in 65-nm CMOS, with a total $P_{DC}$ = 59.9 mW in a size of 15 cm$^3$ [24]. (b) Photograph of the published CSAC "SA65s," a commercial Rb CPT-based clock from Microchip with a total $P_{DC}$ = 120 mW in a size of 17 cm$^3$ [25]. (c) Photograph of the published "mRO"[1], a commercial miniaturized Rb clock from Safran based on double-resonance spectroscopy, with a total $P_{DC}$ = 350 mW in a size of 50 cm$^3$ [26].*

Fig. 3 shows a few photographs of published CSACs along with their corresponding volumes. On all of the pictured PCBs, the physics packages can be clearly identified as the taller, vertically oriented structures mounted on the board. The remaining PCB area is populated with electronics related to DC power generation, control circuits, and the RF synthesizer chain. As of 2024, there are several commercial companies offering CSAC products[2] such as Microchip [27], Teledyne [28], Taitien [29], and Safran [30].

The IEEE time-domain metric for an oscillator's frequency instability is defined as a two-sample deviation called the Allan deviation (ADEV), $\sigma_y(\tau)$ [31], [32], [33]. For example, the commercial Microchip "SA65" CSAC cites an ADEV of $\sigma_y = 3.0 \times 10^{-10}$ at a $\tau$ = 1-s time interval [27]. This means that between two measurements separated by 1 s, there has been 0.003-Hz root mean square (rms) of frequency deviation from the nominal 10-MHz output. Fig. 4 shows a comparison of ADEVs versus integration time for a few different physically

[1]Trademarked.

[2]Certain equipment, instruments, software, or materials are identified in this article in order to specify the experimental procedure adequately. Such identification is neither intended to imply recommendation or endorsement of any product or service by NIST, nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose.

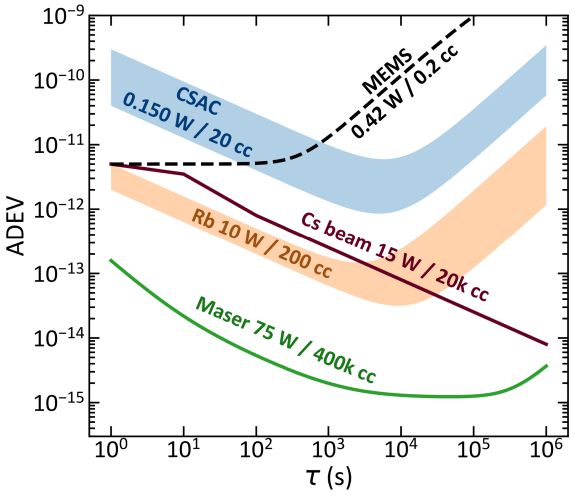


**Fig. 4.** ***Comparison of common commercial atomic clock technologies. The clock performance (here shown as fractional frequency stability (ADEV) versus integration time $\tau$) and drift rates generally improve as power consumption (W) and size ($cm^3$) increase. The shaded regions for CSACs and Rb vapor cell clock indicate the range of published performances. Recent advances in MEMS clocks are presented for context.***

compact and relatively lower power frequency standards, including CSACs, Rb vapor cells, oscillators based on micro-electromechanical systems (MEMS), cesium beams, and hydrogen maser clocks. It can be seen in Fig. 4 that CSACs are still largely outperformed by larger and more power-hungry frequency standards by a few orders of magnitude, which limits their use to low-power applications that can still operate with less precise clocks. To address this issue, new architectures and advancements to existing CSACs are being developed [34], [35], [36], [37], [38], [39], which show promise for better short-term ($\tau \sim 1$ s) and long-term ($\tau > 1000$ s) stability. As these new clocks gain stability improvements through either systematic refinement or new atomic interrogation schemes, they can become limited by low LO performance, and this must be addressed to further improve the overall frequency stability for future microwave CSACs.

In this article, we review and comment on the design, implementation, and performance of existing LOs developed specifically for low-power, CSACs. The requirement of low DC power consumption and high performance in a complex, compact system necessitates unique LO designs with improvements to efficiency, integration, and frequency stability. First, we review how each of the LO metrics affects the total clock metrics, such as frequency stability and power consumption. Then, a state-of-the-art comparison table of published CSACs and their constituent LOs is presented. Potential improvements to the future design of LOs for CSACs are then examined. Finally, we briefly discuss the landscape of other miniaturized frequency references, including advances in miniaturized molecular, small atom beam, trapped ion, and optical clocks.

## II. RF LO METRICS FOR CLOCKS

In this section, we review how the performance of the microwave LO affects the overall clock metrics, including frequency stability, power consumption, and the phase noise of the clock output signal. First, it is important to understand how the stability of a free-running oscillator changes compared to the stability after locking to the atomic resonator. Fig. 5 shows how the ADEV of a free-running oscillator is, somewhat surprisingly, typically better than that of the atoms at low integration times, but starts increasing after some time ($\tau = 10^2$ s in the example) due to random walk FM, frequency shifts, and other environmental shifts such as pressure, temperature, and aging [40]. Conversely, the ADEV of the atoms is often initially worse than the free-running LO, and afterward generally improves with some $\sqrt{\tau}$ dependence, providing orders of magnitude improvement over the free-running oscillator at long integration times. Based on these stability traces, for the most stable clock possible at short- and long-term integration times, an appropriate lock time must be chosen to lock the LO to the atomic resonance line ($t_{\mathrm{lock}}$) at the integration time at which it becomes more unstable than the atoms. This allows the system to take advantage of the best stability from the free-running oscillator and the atoms.

Importantly, Fig. 5 also shows how the choice of $t_{\mathrm{lock}}$ can degrade the stability of the clock, even when using the same high-performance LO. In addition to frequency stability considerations stated here, figures of merit (FoMs)

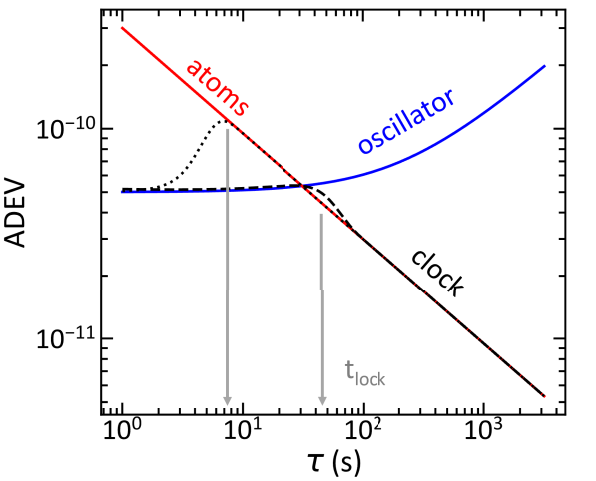


**Fig. 5.** ***Example stability of a drifting oscillator disciplined by an atomic clock. Here, the oscillator (blue line) has good short-term stability but drifts at long integration times, and the atoms (red) have relatively poor short-term stability but do not drift. The integration time ($t_{lock}$) at which feedback acts on the oscillator can impact clock performance, as shown in the dotted (shorter $t_{lock}$) and dashed (longer $t_{lock}$) lines.***

related to the LO, such as size, power consumption, and output power, are often at odds with each other, resulting in complex tradeoffs for any LO design.

### A. Effects of LO Phase Noise, Stability, and Modulation on Total ADEV

Microwave oscillators can be simplistically modeled using an ideal gain element, such as an amplifier, connected to a resonant circuit, which determines the oscillation frequency, $\nu_0$. Ideally, this oscillator operates as a DC-to-RF converter, producing an impulse function at a single frequency. In reality, oscillators exhibit spectral broadening in the form of phase noise due to circuit- and device-related noise sources. To the first order, the phase noise of such a free-running microwave oscillator can be explained by the Leeson [41] effect. A well-known conclusion of Leeson's linear time-invariant (LTI) phase-noise model is that an increase in the loaded resonator quality factor ($Q_L$) will provide a quadratic improvement in phase noise $\mathcal{L}(f)$ as

$$\mathcal{L}(f) = 10\log_{10}\left[\frac{FkT}{2P_s}\left(1+\left(\frac{\nu_0}{2Q_L f}\right)^2\right)\left(1+\frac{f_c}{f}\right)\right]. \tag{1}$$

Here, $\mathcal{L}(f)$ is the single-sideband noise power spectral density (PSD) in dBc/Hz, which is related to the phase-noise PSD $S_\varphi$ in dB $\cdot$ rad$^2$/Hz by $\mathcal{L}(f) = 1/2S_\varphi(f)$, $F$ is an empirical noise parameter of the device, $k$ is Boltzmann's constant, $T$ is the temperature in Kelvin, $P_s$ is the power dissipated in the resistive element of the resonator, $\nu_0$ is the oscillation frequency, $Q_L$ is the loaded $Q$-factor of the resonator, $f$ is the frequency offset from the carrier, and $f_c$ is the flicker corner of the active device.

Many publications have shown that the phase noise of the LO at specific frequency offsets, related to the atomic interrogation scheme, can limit the clock's total frequency stability [10], [42]. The two major effects of LO phase noise that limit the achievable clock frequency stability are described by the "Dick effect," which is an aliasing effect for systems using pulsed interrogation schemes, and the "intermodulation effect" for continuous interrogation [42] [43]. These effects arise from a nonlinearity caused by the atomic resonator interrogation process, which exists in many types of passive frequency standards [44]. This nonlinearity causes frequency translation of spectral noise in the LO output into the frequency bands of the atomic resonator response. In this article, we mainly focus on the intermodulation effect specific to continuous interrogation schemes, as these are more prevalent in this article on chip-scale clocks. The formulation of the intermodulation effect is dependent on the modulation frequency $f_m$ and the type of modulation function $g(t)$, which is used to scan the atomic resonance line [45], [46]. The most commonly used sinusoidal and square-wave modulation functions are, respectively, given by

$$g(t) = \begin{cases} m\cdot\sin(2\pi f_m t), & \text{for sinusoidal modulation} \\ m\cdot\operatorname{sgn}(\sin(2\pi f_m t)), & \text{for square-wave modulation} \end{cases} \tag{2}$$

where $m$ is the modulation depth. The generic formulation and derivation of the intermodulation effect can be found in [10]. For the two common cases in (2), the limits on total clock frequency stability due to the phase-noise PSD of the LO output are given by

$$\sigma_{y\mathrm{LO}}(\tau) \approx \sqrt{\left(\frac{f_m}{\nu_0}\right)^2 \cdot \frac{S_\varphi(2f_m)}{4}}\cdot\tau^{-1/2} \tag{3}$$

$$\sigma_{y\mathrm{LO}}(\tau) = \sqrt{\sum_{n=1}^{\infty}\left[\frac{f_m}{\nu_0}\cdot\frac{2n}{(2n-1)(2n+1)}\right]^2 S_\varphi(2nf_m)}\cdot\tau^{-1/2} \tag{4}$$

where $\sigma_{y\mathrm{LO}}$ is the limit on the total clock stability due to the LO evaluated at an integration time ($\tau$), $f_m$ is the LO modulation frequency, $\nu_0$ is the fundamental RF of the LO, and $S_\varphi$ is the phase-noise PSD of the LO output in rad$^2$/Hz, keeping in mind the commonly used phase noise $\mathcal{L}(f)$ in (dBc/Hz) is related by $\mathcal{L}(f) = 1/2S_\varphi(f)$. Equation (3) is for sinusoidal modulation, and (4) is for square-wave modulation.

The intermodulation effect reviewed here requires a quasi-static assumption $f_m \ll \Delta f$, where $\Delta f$ is the linewidth of the atomic reference line. For any atomic passive frequency standard, the choice of $f_m$ has an upper bound determined by the width of the atomic reference line, and a lower bound determined by the $1/f$ noise in the detection system. Within these bounds, the $f_m$ is typically chosen to minimize the effect of the LO phase noise on the total ADEV, determined either theoretically based on the equations above or experimentally for a specific clock. As a theoretical example, applying (3) and using an arbitrary $f_m = 1$ kHz, a short-term stability limit of $\sigma_y = 1\times10^{-12}$ at $\tau = 1$ h can be achieved as long as the LO phase noise $\mathcal{L}(f)$ is below $-68$ dBc/Hz at a 2-kHz offset from a 4.6-GHz carrier frequency.

The effects of LO phase noise on clock stability for pulsed interrogation schemes, although not as popular in current CSACs, can be described by the Dick effect shown for convenience in the following equation:

$$\sigma_{y\mathrm{LO}}(\tau) = \sqrt{\frac{1}{\nu_0^2}\sum_{n=1}^{\infty}\left[\frac{\sin(n\pi T/T_c)}{n\pi T/T_c}\right]^2 (2nf_s)^2 S_\varphi(2nf_s)}\cdot\tau^{-1/2} \tag{5}$$

where all other variables are the same as (3) and (4), with $f_s$ being the sampling frequency and $T/Tc$ being the dead

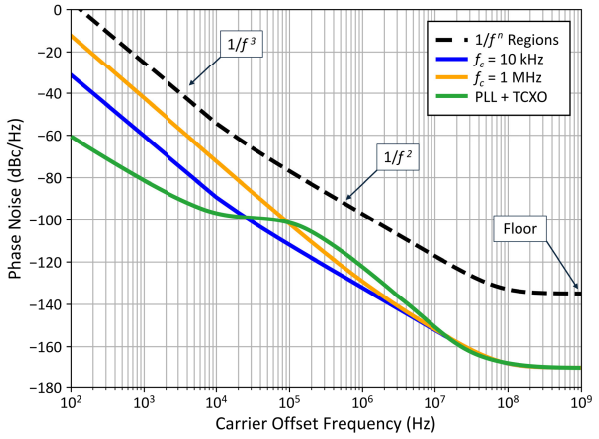


**Fig. 6.** *Qualitative phase noise $\mathcal{L}(f)$ profiles comparing two free-running 4.6-GHz microwave oscillators with different corner frequencies, where $f_c = 1$ MHz corresponds to the order of magnitude for HEMTs and FETs, while $f_c = 10$ kHz corresponds to oscillators with bipolar devices such as SiGe or InGaP/GaAs HBTs. The profiles are calculated using Leeson's equations. The dashed line indicates the $1/f^n$ regions as a guideline. The green curve is a qualitative profile for a PLL-stabilized oscillator using a quartz crystal. Other variables in Leeson's equations are kept the same for comparison (Q-factor, RF power, carrier frequency, noise factor, and temperature).*

time between cycles. Additional research on the Dick effect specific to pulsed CPT-based clocks can be found in [47].

To help exemplify why these equations are important for determining the LO specifications, a sketch of some example phase-noise profiles for a generic 4.6-GHz microwave LO is shown in Fig. 6. The dashed line corresponds to a phase-noise profile of a free-running oscillator described using Leeson's equations, which provide a useful model for the phase noise of an LO based on its $Q$-factor and flicker corner frequency [41]. The flicker corner frequency $f_c$ tied to the inherent LO semiconductor properties separates the white phase noise from flicker phase noise and other progressively increasing noise slopes $(1/f, 1/f^2, 1/f^3, \ldots,)$ at lower offset frequencies [48]. The two other Leeson's phase-noise profiles compare free-running microwave oscillators with different corner frequencies, where $f_c = 1$ MHz corresponds to the order of magnitude for high-electron-mobility transistor (HEMTs) and field-effect transistor (FET) devices such as in CMOS or GaN technologies, while $f_c = 10$ kHz corresponds to oscillators with bipolar devices such as silicon bipolar, SiGe, or InGaP/GaAs heterojunction bipolar transistors (HBTs) [49], [50], [51]. The green curve is a qualitative profile for a PLL-stabilized 4.6-GHz VCO locked to a relatively more stable 10-MHz quartz oscillator, reducing the phase noise at low-frequency offsets below an arbitrary loop filter bandwidth of 10 kHz. This is highly relevant for improving the overall atomic clock stability, as general offsets below 10 kHz have a dominant effect on the stability performance, as explained previously.

On top of the intermodulation and Dick effects, the microwave LO also has a general stability requirement based on the low-offset phase noise. This requirement is typically for phase-noise offsets around 1 Hz, which corresponds to the ADEV at 1 s, and therefore, one should consider if this limits the stability of the overall clock. Furthermore, low-performing LOs can exhibit high temperature sensitivity or large phase-noise slopes below 100 Hz, which would make locking to an atomic cell difficult and possibly change the required locking bandwidth to the atoms.

For some practical published examples of how LO phase noise and modulation scheme can affect the total frequency stability in CPT-based vapor cell CSACs, the LO in [52] has a measured phase noise of $-85$ dBc/Hz at 2-kHz offset frequency and a corresponding measured ADEV for the clock of $\sigma_t = 5 \times 10^{-11}$ at 1 s when modulated with a square-wave modulation function of $f_m = 1$ kHz. In [24], the phase noise $\mathcal{L}(f)$ of the VCO is $-62$ dBc/Hz at $2f_m$, and this gives a total short-term stability for the clock of $\sigma_t = 6.71 \times 10^{-11}$ at 1 s using a square-wave modulation function of $f_m = 71.4$ Hz. Both LOs were implemented using integrated CMOS PLLs locked to a quartz VCXO, which consumed only 10–20 mW of DC power.

## B. Effects of LO Output Power on ADEV

In addition to LO phase noise, the LO RF output power can also limit the frequency stability of atomic clocks, depending on the architecture. In CPT-based atomic clocks, for instance, frequency modulation of the VCSEL can induce light shifts that can degrade the overall frequency stability. Typically for these types of clocks, the LO modulates the VCSEL at either full or half of the ground-state hyperfine transition frequency for the atomic species. In the first case, the carrier and a first-order sideband are used to drive the targeted transition, and the LO RF power controls the relative strength of the relevant optical fields. In the second case of the half-hyperfine frequency, two first-order sidebands separated by the full-hyperfine frequency drive the transition. In this case, the LO RF output power controls the power balance between the resonant and off-resonant optical fields. In both cases, frequency instability at the clock output can be generated through variation of the RF power [53], [54], and operational LO powers can be identified that reduce the clock sensitivity to overall optical power. Fig. 7 shows an example of the optical frequency spectrum of the VCSEL for both modulation schemes, with the RF LO power controlling the strength of the relevant sidebands.

The specific values of these powers are subject to each individual atomic interrogation scheme, but are often on the order of $-5$ to 10 dBm of RF power for CPT-based CSACs using VCSELs [2]. In summary, the atomic interrogation process requires variable RF output power control and output power stability, which can be done in numerous

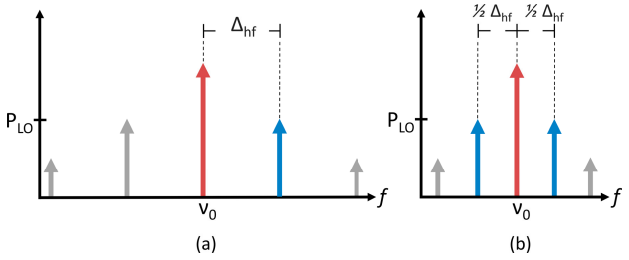


**Fig. 7.** *Sketch of the optical frequency spectrum of a VCSEL while being frequency-modulated by a microwave LO in a CPT-based atomic interrogation scheme. $P_{LO}$ is the RF output power of the LO, which controls the relative strength of the optical sidebands. (a) Sketch of the optical carrier and first-order sideband separated by the full-hyperfine transition frequency and (b) two first-order sidebands each separated by half of the hyperfine frequency.*

ways, such as VCO supply modulation, buffer-amplifier supply modulation, or controllable attenuators, and is discussed in Section IV.

## C. Effect of LO on Total Clock DC Power Consumption

Another FoM especially important for the low SWAP-C applications of small atomic clocks, differing from their physically larger more frequency-stable counterparts, is the total DC power consumption ($P_{\mathrm{DC}}$). A significant percentage of this total power is often dedicated to the LO chain used to generate the atomic interrogation signal. Fig. 8 shows the $P_{\mathrm{DC}}$ for a few integrated microwave LOs compared to the total $P_{\mathrm{DC}}$ of their respective clock systems. For instance, in [24], the microwave LO and driving circuits account for ≈23.5 % of the total $P_{\mathrm{DC}}$ (59.9 mW), with over 11.2 mW for the LO/driver and an additional 2.9 mW for the VCXO in the PLL. In [55], the prototype clock system consumes 42 mW (without vacuum and heating circuits), with the LO chain consuming >50% of the total power (26 mW). In most CSAC implementations, the peak power consumption for the microwave LO is dictated by the RF output power requirements for the optimal optical sideband power in that respective system, which sometimes requires additional high-power amplifier (PA) stages to reach.

Since RF oscillators usually consume more power (higher current) for lower phase noise, and there is a tradeoff between phase noise and conversion efficiency, it is difficult to reduce the LO power consumption below a few mW without sacrificing stability [56]. Efforts have been made to reduce the power consumption from the LO to the furthest extent while maintaining high performance. These include operating the RF VCO in different modes [24], improved VCO circuit architectures [57], new types of high-$Q$ RF resonators [58], new heterogeneous packaging technologies [59], and improvements to the power consumption of PLL circuits, all of which are discussed in Section IV.

## D. Servo Electronics

As explained earlier, the main feedback loop in microwave atomic clocks consists of an RF LO whose output frequency is tuned near the targeted atomic transition frequency, causing the power transmitted through an atomic cell to change. Using CPT-based clocks as an example, the optical power of the VCSEL modulated by an LO is incident on a photodetector, whose output voltage is used to create a feedback signal for the LO to change its output frequency, in what is called a frequency-locked loop (FLL). This is the main servo loop used to discipline the LO to the targeted hyperfine transition, thus creating a relatively long-term stable oscillator. To create this FLL, usually a number of additional control loops are used: a wavelength-locked loop (WLL) that locks the VCSEL optical wavelength to the appropriate optical atomic transition; a second loop to maintain the appropriate VCSEL and atomic cell temperatures; another loop to control the RF LO power incident on the VCSEL; and finally, a PLL to further stabilize the RF VCO and provide a 10-MHz clock output often using a quartz crystal oscillator. The electronics required for these feedback loops are frequently combined in a single application-specific integrated circuit (ASIC), which allows for increased efficiency in a very small footprint. Due to the desire for a high level of integration of all electronics required for a CSAC, including the RF LO, it is worthwhile to briefly discuss how each of these servo loops impact the electronics design as a whole. Significant progress in miniaturizing these electronic control circuits has been shown in recent years, including a number of commercial products [27], [28], [29].

The design of a WLL primarily involves controlling the output wavelength of a VCSEL by adjusting its drive current, which proportionally tunes its wavelength as long as the temperature is stabilized. Using the drive current as a control knob, the optical wavelength can be locked to a point corresponding to maximum

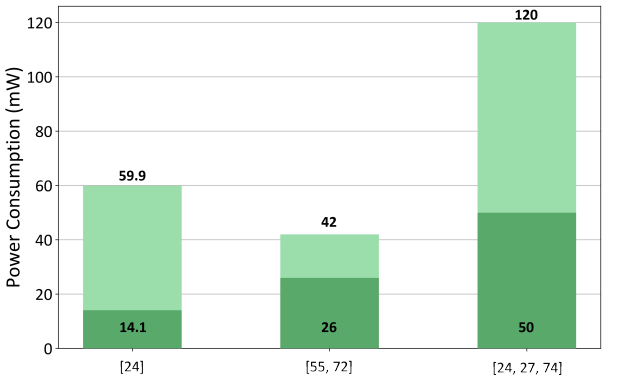


**Fig. 8.** *Comparison of LO and total clock $P_{DC}$ (in bold) for three integrated clock systems in the literature. Zhang et al. [24] do not distinguish between locking circuits and VCO. Haesler et al. [55] do not include $P_{DC}$ related to heating and vacuum systems.*

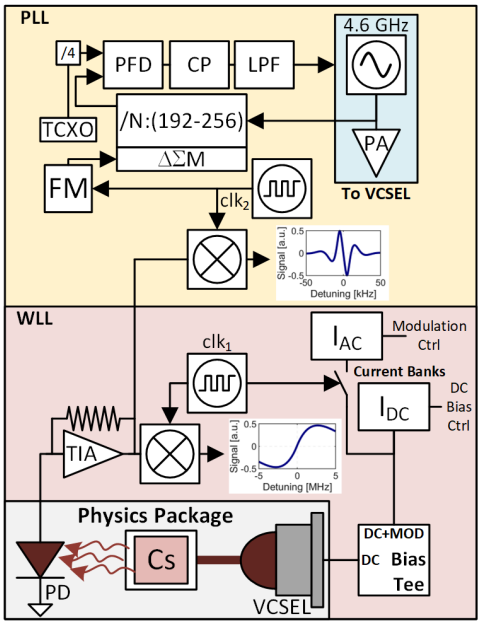


**Fig. 9.** ***Block diagram schematic showing the WLL and the PLL forming servos to control the physics package in a CPT-based CSAC.***

absorption through the atomic cell. To detect this operating point, the DC drive current of the VCSEL is swept in combination with a small AC modulation current that produces two measurement values from the photodetector. The signal can then be demodulated by mixing it with the same AC frequency, generating an error signal. This error signal can then be minimized by adjusting the DC current—incrementing it if the error signal is positive, or decrementing it if the error signal is negative.

An example block diagram of a WLL is shown in the bottom section of Fig. 9. The sensitivity of a typical VCSEL's optical frequency to changes in bias current is around ≈200 GHz/mA, while the linewidth of a collisionally broadened optical resonance in a microfabricated vapor cell is on the order of ≈1 GHz [60]. It is of critical importance that the WLL must be able to lock the VCSEL frequency within the linewidth of the optical resonance. A current source with LN and minimum current steps on the order of a few nA is required to achieve a symmetric lock to the resonant frequency. Such current sources have been realized by using a reference current generator, where the voltage reference is replaced by a digitally controllable voltage source, such as a resistive digital-to-analog converter (R-DAC) [61], [62], or by programming the reference resistor [63], [64]. R-DACs are known to suffer from process, voltage, and temperature variations, which must be accounted for using trimming or calibration. An alternative approach is to generate a temperature-stabilized reference current [65], [66] and mirror the current using a programmable current bank [24]. Noise in the current source, particularly low-frequency flicker noise, can be controlled by the sizing of the transistors. Sensitivity to power supply variations can be controlled by increasing the impedance of the current sources through cascoding.

Use of PLLs in CSACs provides two major benefits for the RF LO: one by providing a means to have a 10-MHz output as to interface with other systems, and second in the improved phase noise of the RF VCO below the PLL filter bandwidth, where the phase noise is most relevant. Often, the frequency control of the LO used in the FLL is tightly integrated within the digital electronics of the PLL, and this can help dictate which PLL architecture is best. For example, due to the relatively narrow width of the atomic response being tuned over in CPT-based CSACs, a frequency resolution of only a few mHz is needed [24]. To achieve this level of resolution, a fractional-$N$ PLL is commonly used, and since there are no practical frequency references that operate down to a few mHz, integer-$N$ PLLs become impractical. An example of a fractional-$N$ PLL is shown in the top portion of Fig. 9 [67]. In most PLL designs, a frequency reference with good short-term stability, such as a temperature-compensated crystal oscillator (TCXO), is input to the PLL consisting of a phase–frequency detector (PFD), a charge-pump (CP), a loop-filter (LF), a VCO, and a divider controlled by a $\Delta\Sigma$-modulator. In the PLL example shown, the fractional division ratio is realized by dithering between two (or more) integer division ratios (e.g., $M = 229$ and $P = 230$) to realize an effective division ratio (e.g., $N = 229.81579425$) that is between $M$ and $P$. The $\Delta\Sigma$-modulator shapes the frequency error with a high-pass response. In terms of phase noise, the PLL has a low-pass response for noise from the divider of the PFD, and a high-pass response for noise from the VCO, where the cutoff frequency is set by the loop filter bandwidth. When optimizing the loop bandwidth of the PLL, there is an optimal bandwidth where noise contributions from the VCO, the $\Delta\Sigma$, and the frequency reference are balanced [68]. In a fractional-$N$ PLL, the reference noise tends to dominate at low frequencies, while the $\Delta\Sigma$-modulator noise and VCO noise dominate at higher frequencies. In terms of control, the frequency resolution of a fractional-$N$ PLL is determined by the number of bits in the $\Delta\Sigma$-modulator where the number of bits, $K$, is given by

$$K = \log_2\left[\frac{f_{\text{ref}}}{f_{\text{step}}}\right] \tag{6}$$

where $f_{\text{ref}}$ is the frequency of the reference oscillator, and $f_{\text{step}}$ is the required frequency resolution.

Finally, in the FLL servo loop used to lock to the atomic response, the VCO frequency needs to be modulated at some frequency $f_m$ before it is applied to the VCSEL. Similar to the mechanism for the WLL, the measurement of two signals that can be demodulated by mixing the recovered signal with the same frequency is used to create an error signal. This error signal can be minimized by incrementing the VCO frequency by changing the divider ratio or the

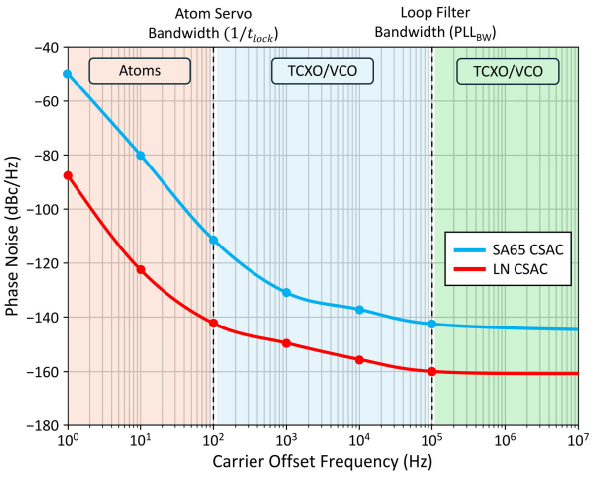


**Fig. 10.** ***Phase noise $\mathcal{L}(f)$ of the final 10-MHz output for the "SA65" and "LN" CSACs commercially available from Microchip [27], [69]. The three colored regions illustrate how phase noise is dominated by different sources: the atoms, TCXO/OCXO, and/or VCO. At low offsets, below the atom servo bandwidth, the phase noise is dominated by the stability of the physics package. At higher frequency offsets, the phase noise is dominated by either TCXO/OCXO or VCO, depending on which is used for the clock output.***

reference frequency by tuning it with a varactor, which is often built-in.

### E. Effects of LO on Clock Output Phase Noise

While ADEV is the central metric for representing a clock's stability in the time domain, it can be useful to examine the same stability in the frequency domain by looking at the phase noise of the final clock output. The output frequencies for clocks are routinely selected to be 10 or 100 MHz to be compatible with most external electronics, much lower than the microwave atom transition frequency of the atomic species used in CSACs. To facilitate this lower frequency output, the signal is regularly taken directly from the TCXO or oven-controlled crystal oscillator (OCXO) within the PLL of the microwave LO, as shown in Fig. 2. Alternatively, the RF VCO operating at the atom transition frequency can be used as the output [12], with additional frequency-division circuits to resolve the lower frequency.

Fig. 10 shows the phase noise $\mathcal{L}(f)$ of the 10-MHz output signals for the "SA65" and "low-noise (LN)" CSACs commercially available from Microchip [27], [69]. In both clocks, the output signal is taken from the quartz crystal oscillator used in the internal PLL, removing the need for additional frequency division circuits. The improved phase noise for the LN-CSAC comes from the use of an OCXO in the PLL compared to the traditional TCXO used in the "SA65," improving the phase noise for a small size and power consumption increase [70]. The shaded regions show how the noise at different frequency offsets is determined to first-order by the atomic stability of the physics package (red) and the TCXO/VCO stability (blue/green). The regions in this frequency-domain plot are analogous to the regions in Fig. 5, represented in the time domain. The width of the region dominated by the atoms is determined by $1/t_{\mathrm{lock}}$, the chosen attack time of the servo loop that stabilizes the LO to the atoms. A distinction between the two TCXO/VCO regions in blue and green at a frequency equal to the PLL filter bandwidth is shown to represent how the phase-noise profile of the clock output can change based on where in the microwave LO the output is taken. For example, if instead an RF VCO within a PLL is used as the clock output instead of a TCXO/OCXO, the clock output phase noise will be determined by the noise properties of the VCO disciplined with the PLL. This could result in a reduction of the higher offset phase noise beyond the loop filter bandwidth compared to the TCXO/OCXO example in Fig. 10, due to the improved phase noise at high-frequency offsets of the RF VCO relative to the TCXO/OCXO, with a similar shape to the "PLL + TCXO" line shown previously in Fig. 6. Some laboratory CSACs discussed in Sections III and V do this and instead use the RF VCO alone as the output, with no PLL or TCXO, and externally stabilize the RF resonator to achieve the required stability.

## III. STATE OF THE ART

The first LOs for CSACs in the 2000's were designed on PCBs using discrete silicon bipolar transistors on physically large substrates, taking up areas on the order of ($>1\,\mathrm{cm}^2$) [79]. This allowed for the use of high-$Q$ resonators that could be integrated on a substrate such as ceramic coaxial resonators, further improving LO phase noise. In the last ten years, the state of the art for LOs in CSACs has been dominated by IC implementations in CMOS or SiGe BiCMOS, using on-chip resonators as a means to save power and volume [52].

Table 1 presents a performance comparison between LOs used in published microwave chip-scale clocks. With the exception of [26], [76], and [77], all use CPT-based interrogation schemes, at a subharmonic of the half-hyperfine splitting frequencies for $^{133}$Cs or $^{87}$Rb atoms, which are around 4.596 and 3.417 GHz, respectively. The types of microwave resonators used in the RF VCO designs range from traditional on-chip inductor and capacitor implementations ($LC$), to external resonators such as quarter-wave ceramic-coaxial resonators or thin-film acoustic MEMS resonators. The latter include thin-film bulk acoustic resonators (FBARs) and high-overtone bulk acoustic resonators (HBARs). Many of these LOs are designed using RF VCOs at the half-hyperfine frequency within a PLL, phase-locked to a more stable VCXO in the MHz range. The PLL filter improves the LO's close-offset phase noise and short-term stability, at a small cost of power consumption and size. All of the listed FoMs in Table 1 are presented, factoring in the entire synthesis chain, including any quartz oscillators, digital circuits, or later amplifier gain stages used in the RF synthesis process. Also, Table 1 shows a list of the measured ADEVs for the complete atomic clock

**Table 1** Comparison of Published RF LOs and ADEVs for Small, Low-Power Microwave Clocks

| LO Freq. (GHz) | RF $P_{out}$ (dBm) | $P_{DC}$ (mW) | Phase Noise (dBc/Hz@Hz) | Volume ($mm^3$) | Tech. | Lock Type / Resonator | $FoM_C$ @1 kHz (dBc/Hz) | $\sigma_y$ @ $10^0$s ($\times 10^{-11}$) | $\sigma_y$ @ $10^3$s ($\times 10^{-11}$) | $\sigma_y$ @ $10^5$s ($\times 10^{-12}$) | Ref. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 4.6 | −8 to 6 | 14.1 | -62 @150 | 1.5x1.7x0.3 | 65-nm CMOS | PLL / LC | *-212.7 | 6.7 | 0.8 | 2.2 | [24] |
| 4.6 | -10 to 0 | 12 | -85 @2000 | 0.7x0.7x0.3 | 130-nm CMOS | PLL / LC | -226 | 5 | 0.8 | N/A | [52], [71] |
| 3.4 | 0 to 10 | 26 | -70 @150 | 2.1x2.3x0.3 | 0.18-$\mu$m CMOS | PLL / LC | -229.9 | 6 | *2.5 | 30 | [55], [72] |
| 4.6 | -6 to -1 | 8.3 | -40@1000 | 1.6x1.6x0.3 | 0.13-$\mu$m SiGe BiCMOS | PLL / LC | -188.4 | *8.5 | N/A | N/A | [73] |
| 4.6 | -10 to 0 | *50 | -75@1000 | *4x4x0.3 | N/A | PLL / LC | *-225.2 | 30 | 1 | *320 | [24], [27], [74] |
| 3.4 | *-15 | 9 | -50 @1000 | 1x0.6x0.3 | 65-nm CMOS | None / FBAR | -210.2 | 2.1 | N/A | N/A | [59], [75] |
| ◇231 | *-9.6 | 71 | -65 @222 k | 1.25x4x0.3 | 65-nm CMOS | PLL / LC | *235.4 | 5.4 | *6.5 | N/A | [76], [77] |
| 4.6 | -3 | 10 | -53 @300 | *10x10x2 | Discrete Si-BJT | None / FBAR | N/A | N/A | N/A | N/A | † [78] |
| 3.4 | -5 | 2.8 | -33 @100 | 7x7x2 | Discrete Si-BJT | None / Coax | -203.2 | 24 | N/A | N/A | [79], [80] |
| 3.4 | *-0.7 | 15 | -70 @150 | 10x10x0.2 | Discrete | Inj. Lock / LC | *-235.8 | 10 | 1 | N/A | [81] |
| 4.6 | 3 to 10 | $> 1k$ | -105 @1000 | N/A | N/A | None / HBAR | N/A | 6.6 | 2 | N/A | [82], [83] |
| 3.4 | N/A | *140 | N/A | 36x23x10 | Discrete | PLL / LC | N/A | 3.66 | 1.65 | N/A | [84], [85] |
| 3 | N/A | N/A | N/A | N/A | Discrete | PLL / LC | N/A | 4 | *1 | *5 | [26], [30] |
| 4.6 | N/A | 60 | N/A | <2000 | N/A | PLL / LC | N/A | 16 | *0.55 | *5 | [12] |
| 3.4 | -15.3 | 3.2 | -67 @300 | N/A | Discrete Si-BJT | None / HBAR | -241 | N/A | N/A | N/A | † [86] |

* Represents Estimated Value Based on Figures — † Not tested with a physics package — ◇ Sub-THz Molecular Clock ($^{16}O^{12}C^{32}S$)

systems at increasing timescales. Comparing these listed ADEVs with the long-term stability of the best OCXOs, CSACs have been shown to have better long-term performance even among rapid temperature changes [87]. However, OCXOs still maintain advantages over CSACs in both phase noise and short-term stability [88].

Some important distinctions come from reviewing Table 1, especially when looking at the relative power consumption and size of each of the LOs related to the chosen technology for fabrication and RF resonator type used. Most of the compact, highly integrated systems are all achieved in CMOS technologies using on-chip *LC* resonators ($Q_u < 40$), phase-locked to VCXOs using an integrated PLL. These CMOS-based clocks represent the state of the art in terms of tradeoffs between size and power consumption while maintaining decent short- and long-term stability. Also seen from the table, other avenues show promise in further reducing LO power consumption metrics through the use of high-$Q$ RF resonators ($Q$ from 300 to 1000 s), eliminating the use of PLLs or VCXOs and therefore the DC power required to operate them.

While promising, these oscillators still have engineering challenges that must be addressed before integration into a full commercial CSAC is possible, namely, shifts in RF caused by temperature and vibration. These topics among others related to the design of the LOs themselves will be discussed in Section IV.

Physically, large LOs bigger than a few square centimeters or power-hungry synthesizers consuming >100 mW are not listed in this table as they are not optimized for the topic of CSACs, with the exception of [82] and [83] in Table 1, which is more focused on the miniaturization of the RF resonator. Beyond this list, there remain many promising alternative ways to generate clean and stable RFs in this range, but they are currently too complex, large, or power-hungry to be implemented in CSACs. Some examples of these alternatives include down-conversion to RF using optical combs [89], [90], multiplication to RF from more stable low-frequency sources using nonlinear transmission lines (NLTLs) or step recovery diodes (SRDs) [5], [91], [92], [93], [94], [95], [96], sampling mixers used to phase lock dielectric resonator oscillators [97], optically stabilized RF oscillators [98], [99], [100], and oscillators involving extremely high-$Q$ resonators cooled to cryogenic temperatures [101], [102], [103]. Depending on future advancements in these fields of research, some

of these methods may become viable for use in a next-generation small, low-power microwave clock.

## IV. RF LOs FOR BETTER CLOCKS

In typical CMOS or SiGe VCO literature, an FoM is used for performance comparisons between designs, factoring in fundamental frequency, phase noise at 1-MHz offset, tuning bandwidth, and DC power consumption [104], [105]. Similarly, VCOs in III–V semiconductors often use an FoM, which accounts for fundamental frequency, phase noise at 1-MHz offset, tuning bandwidth, and output power or efficiency [106], [107]. Most of these FoMs are not as useful for comparisons between VCOs designed for CSACs because they are usually meant to describe utility in communications or radar systems where wide tuning bandwidths and low phase noise at higher frequency offsets are crucial. In contrast to communication systems, wide VCO-tuning ranges and high tuning gains (Hz/V) are not desired in CSACs due to the relatively small target frequency tuning range of the atomic resonator response, which is often on the order of $<$10 kHz. Instead of wide tuning bandwidths, VCOs for CSACs target low phase noise at lower frequency offsets ($<$20 kHz), much lower than the commonly cited 1-MHz offset used in the aforementioned FoMs. Additionally, the typical output power requirements of physics packages discussed in Section II-D require an LO output power on the order of $-5$ to 10 dBm to ensure the lowest instability is achieved when modulating the VCSEL. Therefore, for a given RF output power determined by the physics package, there should be a major importance placed on the overall efficiency of the RF synthesis chain, including subsequent amplification and locking circuits. These complex requirements for properly modulating the VCSEL along with the tight volume restrictions necessitate a slightly more specialized VCO design than can be achieved from commercial off-the-shelf (COTS) systems.

Based on the discussion above, an appropriate FoM for CSACs favors higher RF output power, lower DC power consumption, and lower phase noise at a low offset frequency. Therefore, we choose to adopt an FoM similar to $\text{FoM}_2$ from [107], using a relatively low offset frequency of 1 kHz

$$\text{FoM}_C = \mathcal{L}\left(f_{\text{offset}}\right) - 20\log\left(\frac{f_{\text{osc}}}{f_{\text{offset}}}\right) + 10\log\left(\frac{P_{\text{out}}}{P_{\text{diss}}}\right) \tag{7}$$

where $\mathcal{L}(f_{\text{offset}})$ is the phase noise in dBc/Hz at the specified offset of 1 kHz, $f_{\text{osc}}$ is the LO output frequency in Hz, $f_{\text{offset}}$ is the specified 1-kHz frequency offset, $P_{\text{out}}$ is the RF LO output power in $W$, and $P_{\text{diss}}$ is the total dissipated DC power in W. Each of the FoM entries in Table 1 are calculated using this equation.

Fig. 11 shows a block diagram of a generic microwave *LC* oscillator driving and modulating the injection current of the VCSEL required for creating optical sidebands at the hyperfine frequency of the interrogated atoms in a CPT-based cell. The VCSEL impedance at microwave frequencies is usually complex and can often be a function of temperature and bias current [109]. Impedance matching and coupling the RF VCO to the complex impedance of the VCSEL is a critical step to achieving a low-loss interconnect that compensates for any packaging parasitics of the semiconductor laser, provides a bias-T for DC bias to the laser, and thermally isolates the VCSEL from the oscillator [52].

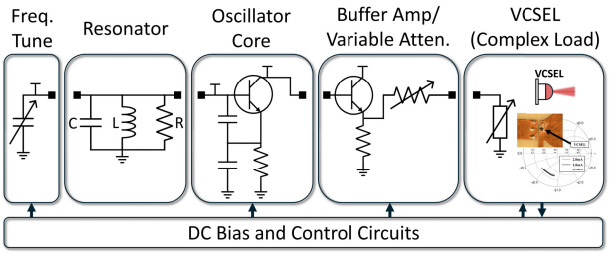


**Fig. 11.** *Block diagram of a generic RF Colpitts VCO using an LC resonant tank for determining the resonance frequency, tunable capacitance via a varactor diode for frequency tuning, transistor with feedback for the oscillator core, buffer amplifier/attenuator for amplitude control and output load pull isolation, and finally, the VCSEL that is a bias- and temperature-dependent load [108]. The rest of the power, control, and feedback circuits are abstractly represented in the following.*

### A. Technology and Integration

Choice of technology for LO design is critical due to its effects on nearly all LO performance metrics and integration with other clock components. In early CSACs, LOs were implemented in low-cost hybrid technologies on large PCB substrates, often using discrete silicon bipolar transistors due to their low $1/f$ noise and moderate size (see [80]). Since then, most LOs for state-of-the-art CSACs have been implemented in ICs using CMOS or SiGe BiCMOS due to their ease of integration with digital control circuits while maintaining reasonable RF performance, as shown in Table 1.

Comparison studies on measured $1/f$ noise in different transistors for ICs and III–V monolithic microwave ICs (MMICs) have shown that HBTs achieve the lowest phase noise at fundamental frequencies relevant to miniaturized clocks [110], [111]. Of the commercially available options, SiGe HBT/BiCMOS [112], [113] and InGaP/GaAs HBT [114] become attractive options for the design of low phase-noise VCOs, with SiGe having the additional advantage of easier integration with CMOS. Due to the output power requirements ($-5$ to $+10$ dBm), a relatively higher breakdown-voltage semiconductor such as InGaP/GaAs HBT provides an advantage as it does not require subsequent gain stages, which consume power and could possibly contribute to the additive (residual) phase noise. This comes at the cost of generally higher power consumption for the VCO individually and more complex integration [115], [116]. Nonetheless, CMOS and

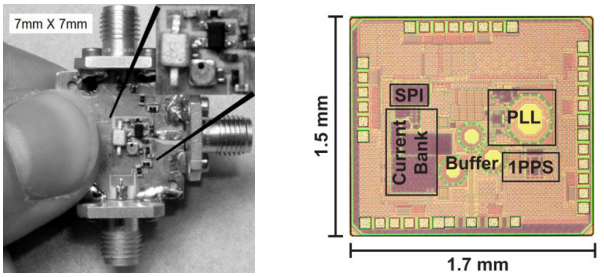


**Fig. 12.** *(a) PCB photograph of a VCO developed for the first CSAC at NIST, implemented on a Rogers substrate with discrete silicon bipolar transistors and a high-$Q$ ceramic coaxial resonator, consuming a few mW of DC power in a 7-mm$^2$ area [80]. (b) Die photograph of an LO developed for the state-of-the-art CSAC called the "ULPAC," integrated on-chip in CMOS taking up less than 1.7 mm$^2$ in area [24].*

SiGe BiCMOS technologies have been used to produce the lowest power commercially available CSACs because of the large importance of integration.

Fig. 12 shows two examples of oscillators designed for use in CSACs. Fig. 12(a) shows a prototype from the earliest CSACs developed at NIST, designed using a ceramic coaxial resonator with $Q \approx 300$ and tested without a PLL. Fig. 12(b) shows a fully integrated IC in CMOS, representing an example of the current state of the art, and contains an *LC* oscillator, PLL, and buffer amplifier on-chip. Both VCOs locked to a miniaturized physics package, resulting in a highly stable and small atomic clock, with the corresponding measured ADEVs listed in Table 1.

## B. Phase Noise, Free-Running Stability, and RF Resonators

The design of low phase-noise RF oscillators has been the subject of many books, articles, and theses throughout the years, resulting in a number of different noise theories with experiments to match [117], [118], [119], [120]. For CSACs, having an LO with good free-running stability and phase noise as described in Section II is imperative for improving the overall clock stability. This free-running phase noise of the LO is largely determined by a combination of the RF resonator $Q_L$, the technology choice as described earlier, as well as the chosen circuit topology.

As stated previously in Section II-A, Leeson's LTI model in (1) is sufficient for discussing the impact of RF resonator $Q$ on VCO phase noise to first order. While it is tempting to maximize the resonator $Q$ at all costs, this desire can often contradict with system SWAP-C requirements due to an RF resonator's relationship to its wavelength [121]. Furthermore, most systems require some tuning range, which is often achieved with lossy on-chip varactor diodes, decreasing the realistically achievable $Q$ [122].

Fig. 13 shows a few examples of small RF resonators used in VCOs for published CSACs including an integrated *LC* resonator, a FBAR, and an HBAR. Of these examples, *LC* and microstrip resonators are by far the most common, highly integrated, and straightforward options for VCO design's at these frequencies, providing a planar implementation with a $Q_u$ of normally ≈45 or less and can take up less than 1 mm$^2$ of space [123], [124]. The $Q$-factor limitations of these on-chip resonators are due to radiation, dielectric, and surface resistance loss mechanisms inherent to planar IC designs [125]. Considering off-chip implementations at these frequencies, FBAR and HBAR are both piezoelectric-based acoustic MEMS resonators, which can provide $Q$s in the 1000s or many 10 000s, respectively, in a volume of just a few mm$^2$, at the expense of more complex integration and larger frequency dependence with temperature [126], [127]. Additionally, HBAR resonators present challenges due to their over-moded nature as they require supplementary filtering and gain stages for operation, increasing the size and complexity [128]. Surface acoustic wave (SAW) resonators have become a mainstay in RF applications below ≈3 GHz, but are increasingly difficult to manufacture for higher frequency ranges due to limitations in the miniaturization of interdigital transducers [129]. Beyond these options, there exist a number of high-$Q$ resonators in this frequency range that will not be discussed in detail due to their size, temperature dependence, or technology readiness level. Some examples include dielectric resonant oscillators (DROs) [130], larger traditional high $Q$ cavities [131], whispering-gallery mode

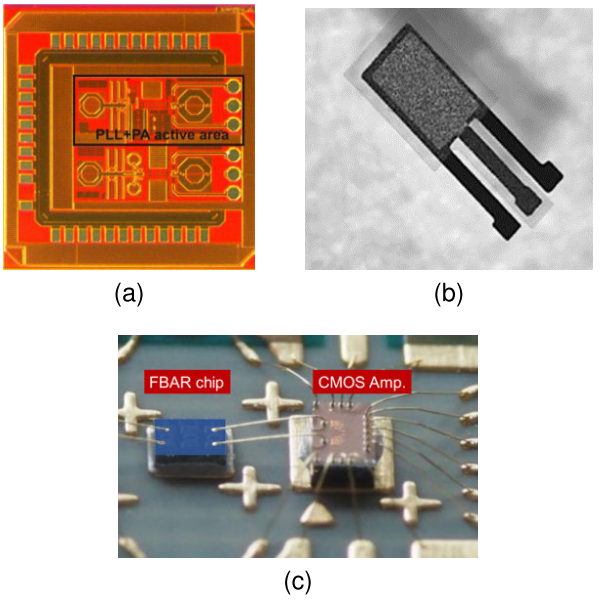


**Fig. 13.** *(a) Die photograph (0.7 mm$^2$) of a fully integrated 4.6-GHz LO in CMOS for a CSAC including a VCO using an on-chip LC resonator, PLL, and PA. LC resonators in CMOS typically have an unloaded $Q$ of $Q_u < 40$ [52]. (b) Photograph of an HBAR resonator ($< 1$ mm$^2$) with $Q_u = 19\,000$ used in a hybrid CSAC prototype oscillator [86]. (c) Photograph of an FBAR resonator ($< 1 \times 0.67$ mm$^2$) with a $Q_u = 1100$ integrated with a CMOS oscillator for use in a low-power PLL-free CSAC [59].*

resonators [132], miniaturized loop-gap resonators [133], [134], spoof surface plasmon resonators [135], and ultra-thin 3-D resonators in photo-etchable glass [136]. Progress in the practical application of any of these technologies could lead to large improvements in phase noise for VCOs in CSACs.

Along with choosing a low flicker corner semiconductor technology and improving resonator $Q$, circuit design techniques leveraging insights from time-variant phase-noise theories can allow for further improvements to cyclostationary phase noise [137], [138]. Some examples of these circuit topologies include balanced or differential Colpitts [105], [139], [140], Class-C harmonic [141], tail current-shaped [142], and $G_m$-boosted [143] VCOs, which provide improved phase-noise performance often with the tradeoff of increased complexity or potential start-up difficulties. A few of these circuit topologies have already been leveraged in CSAC systems [24], [71]. In addition to improvements from these generic circuit architectures, component-level design practices such as reducing varactor modulation and DC biasing noise can also have a large impact on reducing VCO phase noise [144]. For example, due to the relatively small (<10 kHz) required VCO-tuning range set by the atomic resonance line, VCOs in CSACs have the advantage of only necessitating a low tuning gain $K_{\mathrm{VCO}}$ (MHz/V), which can help to lessen varactor modulation-induced noise. Practically, the tuning gain should not be too small as to account for systematic frequency deviations from the desired hyperfine frequency. Use of low current noise DC supplies such as batteries or LN linear dropout regulators (LDOs) along with constant current supply circuits like current mirrors or operational amplifiers can also help reduce DC bias noise as much as possible [145].

### C. RF Output Power, RF Amplifiers, and VCSEL Matching

As discussed in Section II-D, the LO needs to provide an RF power level to the VCSEL around −5 to +10 dBm that can be finely controlled based on requirements set by the individual VCSEL, interrogation scheme, and physics package design. To achieve this range of tunable power levels, LOs commonly use either a digitally controlled DC bias of an RF amplifier or variable attenuator at the output of the RF VCO, as shown in Fig. 11, which also provides a buffer from potential frequency load-pulling [12], [24], [146]. This digital control of the output power can then be easily interfaced with the rest of the digital and feedback control circuits. While these are relatively standard solutions implemented in RF synthesizers, challenges arise for LO designers when trying to maximize the tradeoff between efficiency of the RF synthesis chain and maintaining a suitable phase-noise metric [116]. This can be especially true if the RF VCO output power is well below the desired range, as further amplification stages are required, which place a larger emphasis on the additive phase noise of the amplifier stages. RF amplifier phase

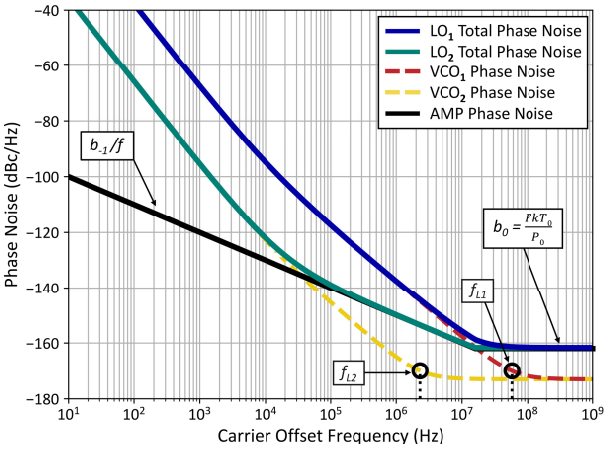


**Fig. 14.** *Example of the effects of additive phase noise for an RF PA (AMP) operated in mild compression, amplifying the output of a generic 4.6-GHz VCO in two cases. $VCO_1$ represents an oscillator with an LC resonator with $Q_L = 40$ and $VCO_2$ using a high-Q RF resonator with $Q_L = 1000$. The resulting total LO phase noise is found by adding the amplifier, and VCO phase noise in each case is shown, with degradation at medium-to-high-frequency offsets. The Leeson frequencies, $f_L$, are also shown.*

noise has been demonstrated to be the summation of terms related to white phase noise and flicker noise, written in [147] as

$$S_\varphi = b_0 + \frac{b_{-1}}{f} \quad \left[\mathrm{rad}^2/\mathrm{Hz}\right] \tag{8}$$

where the term $b_{-1}$ is the flicker coefficient of the amplifier, which is primarily determined by the semiconductor technology. The white noise term $b_0$ is defined as

$$b_0 = \frac{FkT_0}{P_0} \quad \left[\mathrm{rad}^2/\mathrm{Hz}\right] \tag{9}$$

where $F$ is the amplifier noise figure, $P_0$ is the input RF power to the amplifier, $k$ is Boltzmann's constant, and $T_0$ is the temperature in Kelvin.

A generic example of how this formulated additive phase noise of a high-efficiency PA can degrade the total phase noise of the LO is shown in Fig. 14. The amplifier shown here is assumed to have a flicker noise component of $b_{-1} = -90$ dBc/Hz and a noise figure of 2 dB in compression while being driven with an input power of −10 dBm from a VCO, which is reasonable given most CSAC LOs are designed in relatively low-power CMOS technologies. In Fig. 14, there are also Leeson phase-noise profiles for two different 4.6-GHz VCOs with identical characteristics except for $Q_L$, with $VCO_1$ using a high-$Q$ resonator of $Q_L = 1000$, which is a reasonable value that could be accomplished with some of the off-chip resonators reviewed previously, and $VCO_2$ with $Q_L = 40$ representing a value using a simple on-chip *LC* resonator. The

corresponding total output phase noise for each of these VCOs is represented by $LO_1$ and $LO_2$. Additionally, the Leeson frequency $f_L = \nu_0/2Q_L$ is provided for added context [148]. Because the low-frequency offset phase noise of the LO (<20 kHz) is often the region of interest due to the Dick/intermodulation effects, it can be seen here that the effect of the amplifier's additive phase noise on the total LO performance depends mostly on the $b_{-1}$ flicker noise term for the amplifier relative to the low offset phase noise of the VCO. Fig. 14 also shows that when using these $Q$-factors, the added noise from a highly efficient amplifier can be mostly neglected at low-frequency offsets (<20 kHz) as long as the flicker noise ($b_{-1}$) of the amplifier is sufficiently low when operated in compression. For higher performing LOs using low phase-noise quartz crystal oscillators in a PLL or high-$Q$ external resonators, the additive flicker noise of a highly efficient amplifier could likely limit the LO phase noise. Commonly, the VCO and the amplifier gain stages are implemented on-chip with a PLL in a single semiconductor process, meaning the VCO and amplifier will have similar flicker noise characteristics.

Notably, some experimental evidence has shown marginally efficient amplifiers driven into mild compression can maintain their low-flicker ($b_{-1}$) performance independent of output power [149]. Nonetheless, the effects on the ($b_{-1}$) flicker noise for different kinds of highly nonlinear, efficient amplifiers has not been well-studied to the authors' knowledge and, in many cases, has shown degradation in the ($b_{-1}$) flicker noise region based on how the amplifier is operated [150], [151], [152], [153]. The use of a highly nonlinear amplifier will still result in degradation in the white noise ($b_0$) region of the LO due to the increased noise figure, which could potentially be relevant.

Beyond analyzing the amplifier's additive phase noise, emphasis should also be placed on determining the impedance of the load driven by the LO at the hyperfine frequency, in this case the VCSEL, and matching this impedance to the LO output. This will provide maximum RF power transfer to the VCSEL, reducing further unnecessary loss. Previous works have shown that the VCSEL impedance can be marginally sensitive to bias current and temperature, which should be accounted for when designing a matching structure [108]. An example of a calibrated impedance measurement for a VCSEL is shown in Fig. 15, showing the complex RF impedance of a 795-nm VCSEL from 3 to 4 GHz across a range of bias currents.

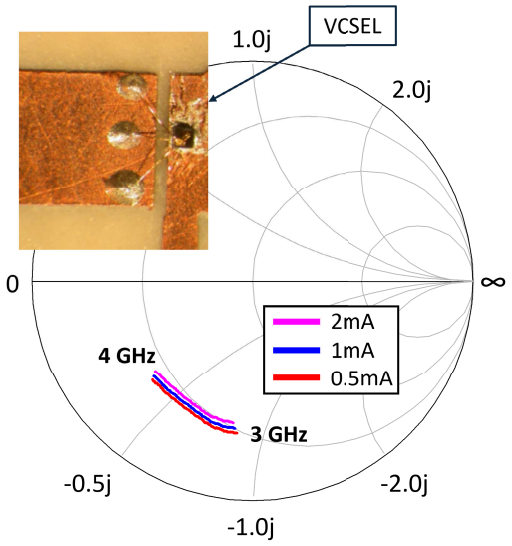


**Fig. 15.** *Calibrated RF impedance measurement of a VCSEL from 3 to 4 GHz for multiple DC bias currents, showing a complex measured impedance plotted on a 50 Ω Smith chart [108] At 3.4 GHz, the impedance at the wirebond reference plane is $Z = 16 - j32\,\Omega$.*

## D. Control Electronics

PLLs have become nearly ubiquitous in RF synthesizers, especially in high-performance situations where stability is imperative. Namely, improvements in calibration for all digital PLLs (AD-PLLs) have enabled significantly reduced footprints [154], which coupled with the enhanced noise performance help enable fully integrated CSACs [24]. Exciting opportunities for future implementations are the use of frequency multipliers and multiplying delay-locked-loops (DLLs) that are currently achieving outputs near 10 GHz, which could be used to drive the atomic transitions [155], [156]. Sub-THz PLLs implemented in CMOS have demonstrated promise for chip-scale molecular clocks operating up to 231 GHz. This was achieved using a 28.9-GHz VCO locked to an 80-MHz VCXO, which was then multiplied to reach the sub-THz transition frequency, all while maintaining a power consumption of less than 80 mW [77].

Because the output frequency of a CSAC is typically generated using a quartz crystal within a PLL, its frequency stability is fundamentally limited by the crystal's short-term stability, which typically does not exceed $1 \times 10^{-13}$ at 1 s for TCXOs [1]. To help improve the clock's short-term stability, emphasis could be placed on finding more accurate, low-power, portable 10-MHz sources, such as MEMS or low-power OCXOs [23], [70].

## E. Power Consumption and Efficiency

The total power consumption and efficiency of the microwave LO are discussed last here due to its dependence on nearly all of the previously mentioned design considerations. Often, the resulting total power consumption of the LO is merely an amalgamation of tradeoffs from previous design choices such as the RF output power requirements and selected technology. Nonetheless, it is one of the most critical performance metrics for consumers as CSACs are often desired in portable, battery-operated systems, where DC power comes at a premium. As such, a significant amount of the LOs in CSACs are focused on reducing the power consumption or increasing the

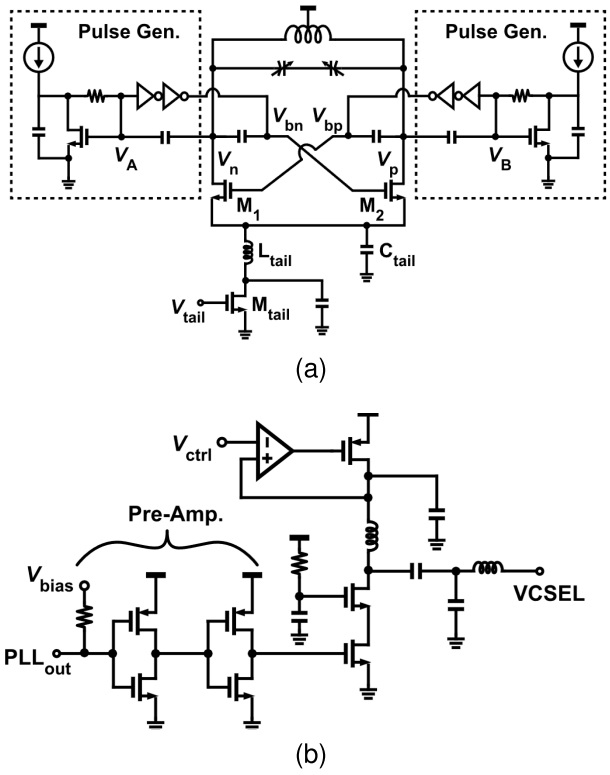


**Fig. 16.** *(a) Example of a pulse VCO as a part of the LO in the "ULPAC" [24]. This VCO architecture uses cross-coupled transistors with waveform shaping via DC bias to increase the DC-to-RF efficiency with the penalty of increased complexity. (b) VCO output is then fed into a digitally controllable (−8 to 5.8 dBm) class-E switch-mode PA with a peak efficiency of 47.3%.*

efficiency of the RF VCO and any RF amplifiers as much as possible through circuit design techniques, while trying to maintain decent phase-noise performance. Fig. 16(a) shows an example of a low-power RF VCO architecture referred to as a pulse VCO as a part of a modern CSAC [24], [157]. This low-power oscillator is then fed through a programmable class-E PA shown in Fig. 16(b), additionally acting as a buffer amplifier, with a peak power efficiency of 47% and peak output power of 5.8 dBm, allowing for a digitally controllable RF power level delivered to the VCSEL. Other than this specific example, there are numerous VCO architectures designed for many different frequency ranges, which may provide a benefit in future CSACs. These VCOs leverage output waveform shaping, dynamic biasing, and current reuse techniques, which can result in very low-power or high-efficiency VCOs with increased complexity or slightly degraded phase noise [158], [159], [160], [161], [162]. Other than increasing the DC-to-RF VCO efficiency, there remain a number of power-added efficiency (PAE), enhancing amplifier architectures that could result in a narrowband, low-power, low-additive phase-noise gain stage [163].

Beyond circuit design improvements, reducing the total LO power consumption depends on creating an effective link budget for the RF power required to drive the VCSEL, as well as the additive phase noise and PAE of any additional RF amplifiers that may be needed. When designing a very low power consumption and low RF output power VCO, and amplifying that output signal using highly efficient switching PAs, one must still consider the effects of the additive phase noise of those efficient amplifiers and ensure the total phase noise of the LO is below the limits determined by the Dick or intermodulation effects.

## V. DISCUSSION AND CONCLUSION

The next-generation microwave CSACs employing different basic principles beyond currently commercialized CPT-based vapor-cell CSACs are being developed by a number of institutions to overcome fundamental limitations of the current architectures [1], [164]. Some of these alternative interrogation schemes include: miniaturized cesium beams [34]; using the Ramsey-CPT method to interrogate the atoms at separated time intervals by utilizing a complex pulsed laser drive current modulation [165]; double resonance in alkali atoms that resulted in a commercial product [30]; THz rotational transitions in molecular gases [77]; and trapped ions in ytterbium or mercury [166]. Most prototypes are focused on reducing the size of the atomic cell, and use a large rack-mounted or off-the-shelf synthesizer, which does not meet SWAP-C for a small clock.

New types of CPT-based atomic interrogation schemes, such as a 25 $\times$ 195 $mm^3$ chip-scale beam clock [34], [36], [167], are under investigation with a projected stability limit of $\approx 9 \times 10^{-12}/\sqrt{\tau}$, limited by quantum projection noise. Because this clock targets the standard 3.4-GHz half-hyperfine transition frequency of $^{87}$Rb and has similar RF requirements to vapor-cell CSACs, many of the LOs reviewed in this article could be adapted to this new type of clock.

In recent years, pulsed Ramsey-CPT methods using optical modulation have shown promise for reducing stability limits due to light shifts in microcell CSACs [168]. Previously, this Ramsey-CPT sequencing was achieved at the bench-top level using acousto-optic modulators (AOMs), which are traditionally bulky and result in high power consumption. As a solution, recent experiments using miniaturized alkali vapor cells have been enabled by creating two laser pulses separated in time using complex pulsed laser drive current modulation, removing the need for AOMs while providing a path to practical implementation in existing electronics used in CSACs [169], [170]. Using these techniques, some groups have achieved stability in the $10^{-12}$ range at one day with the possibility for full integration [171].

A promising alternative to CPT-based small clocks is molecular clocks based on rotational transitions using millimeter-wave metal waveguides. For example, the $^{16}O^{12}C^{32}S$ molecular clock that targets a 231-GHz transition is described in [77] and [172]. In this approach, a section of a waveguide (WR-4.3) is filled with $^{16}O^{12}C^{32}S$ molecules and probed using a millimeter-wave LO realized

in a 65-nm CMOS process with a chip-to-waveguide transition. This clock architecture does not require any lasers or accompanying optics and uses low-power heaters and less magnetic shielding, reducing the overall power consumption. The high millimeter-wave frequency also reduces the size of the clock compared to the lower frequency CPT clocks. The performance of this new type of clock with a demonstrated stability of $5.4 \times 10^{-11}$ at 1 s is comparable to current commercial CSACs [76]. A theoretical analysis of chip-scale molecular clock stability, for different molecular gas options, is shown in a recent publication [173].

In terms of miniature trapped-ion standards, $Hg^+$ clocks targeting 40-GHz microwave transitions [174], [175], [176], e.g., the M2TIC prototypes, have reached the $10^{-14}$ stability level in one day with an SWAP of 1.1 L, 1.2 kg, and under 6 W of power, comparable to rack-mounted Cs beam standards. Future integration is planned with a 40.5-GHz synthesizer occupying 1 $mm^2$, made in 65-nm CMOS and operating from a 40-mW DC power supply [177]. $Yb^+$ clocks using microwave transitions at 12 GHz have also been demonstrated after preliminary miniaturization efforts [166], [178], [179], [180], with a cell sizes around $60 \times 60 \times 110\,mm^3$. The microwave signals for these clocks are at present generated using two large synthesizers and a large antenna. A different trapped-ion clock with a smaller (3 $cm^3$) package is still a bench-top prototype, but shows promising stability results [181], [182]. Yet, to reach this performance (stability of $10^{-14}$) in a chip-scale package would require a high-performance 40- or 12-GHz LO, which could dominate the size or power consumption.

Looking past microwave atomic clocks, large-scale optical clocks have continued to set new records for frequency stability, with a potential switch for the definition of the second from microwave to optical standards seeming increasingly likely [183] and [184]. Since the 2000s, large optical clocks have achieved state-of-the-art fractional frequency uncertainties close to $10^{-18}$ [185], orders of magnitude better than microwave clocks due to the higher frequency atomic transitions. While the lowest uncertainties have been achieved with very physically large and stable setups, there has been great initial progress in miniaturized and portable optical clocks, such as the ones based on the two-photon optical transition in Rb. These clocks incorporate microresonator frequency combs for optical frequency division in a small package [37], [186], but are still in early phases. Nonetheless, compact optical frequency standards would have a fundamental advantage in terms of frequency stability, but still have a number of challenges to overcome for commercial miniaturization.

In conclusion, this article reviews microwave-frequency LOs as key components of CSACs and presents an analysis of the impact of the LO on clock stability. The LO used for a microwave CSAC needs to provide a tunable oscillator close to the targeted atomic transition frequency of the chosen atom, at the appropriate RF output power level for a specific physics package, with a low enough phase noise to not destroy the hard-earned atomically defined stability of the clock, all in a low SWAP-C package. This limitation by the LO can begin to be addressed with corresponding improvements to LO phase noise, DC-to-RF efficiency, and new types of control electronics; some of which were reviewed and expanded on in this article. As microwave CSACs continue to improve, the potential for their application in many size and power-constrained environments becomes available. Currently, these applications range from GPS receivers, oil exploration, and the energy grid.

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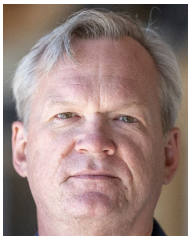

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