FPGA-based Low-Latency Digital Servo for Optical Physics Experiments

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***Abstract*—We propose a general-purpose dual-channel field-programmable gate array (FPGA) based digital servo with a minimum latency around 200 ns. This servo implements a proportional, dual-integration and derivative (PIID) controller along with internal numerical controlled oscillators (NCO), a phase detector (PD) utilizing a fast in-phase and quadrature (I/Q) detection algorithm (80 ns), NCO modulator, network analyzer, auto-locker, ramp generator, and low pass filters. A web interface and/or Python commands over TCP/IP allows full control and monitoring. The servo has been successfully used to lock Pound-Drever-Hall cavities, phase-locked loops and optical frequency combs. A simple experiment phase-locking two dielectric resonator oscillators (DRO) has been set up to demonstrate a 1 MHz closed-loop bandwidth.**

Keywords— automatic locking; digital phase detector; digital servo; DRO; FPGA; low-latency, optical frequency comb

I. Introduction

A servomechanism (servo) is mandatory in almost all feedback systems, and it can accomplish different tasks such as temperature control [1-2], stabilization of frequency, phase and power of lasers and microwave signals [3-4]. Most analog servos have fixed transfer functions with switch selectable circuit components to coarsely tune the frequency response [5]. Depending on the application, various analog modules or instruments must be used to perform phase detection and frequency generation as in a Pound-Drever-Hall (PDH) scheme [6]. Our digital servo allows the user to fine-tune all parameters of the transfer function and can provide additional functionalities as PDs and NCOs. This approach is not new [7-11] and digital servos come with their limitations such as limited bandwidth and signal to noise ratio (SNR) [12]. However, our proposed design tries to lower the total latency without compromising excessively on generality, flexibility and resolution. Thanks to our custom I/Q detection algorithm (80 ns total delay), a fully digital PDH lock is possible up to closed-loop bandwidths around 1 MHz, a result almost impossible to achieve with a standard CORDIC algorithm [17] with same resolution, FPGA fabric and clock speed.

II. Hardware & Software

Our project is based on the Koheron Alpha250 board [13] and the Koheron software development kit (SDK) [14]. This board has 14-bit ADCs and 16-bit DACs running at 250 MSps. It also has slower, high-resolution 24-bit ADCs and 16-bit DACs running at about 40 kHz. The core of the system is a Xilinx Zynq system on a chip (SoC) [15] which has a dual-core ARM processor running Linux and a web server as well as an Artix-7 FPGA. The internal FPGA design runs at 62.5 MHz allowing for phase detection of signals up to 31.25 MHz. Our FPGA design includes two independent PIID controllers for each of the two input/output channels. The main ADCs and DACs have a latency of 24 ns and 32 ns respectively. The minimum FPGA data delay path is 144 ns. Selectable options and associated latencies if any are shown in the following list.

- A selectable first-order input low pass filter (16 ns)
- An optional phase detector (48 to 560 ns)
  - Normal mixing (48 ns)
  - I/Q detection
    - Custom algorithm (80 ns)
    - CORDIC algorithm (560 ns)
  - Phase-Frequency detection (48 ns)
- Adjustable offset
- Another selectable first order low pass filter (16 ns)
- P-I-II-D filter with adjustable gains and offset
- NCO modulator
- Network Analyzer
- Value limiter/clamper
- Optional NCO running at 250 MHz modulable in frequency, phase or amplitude (52 ns)

An additional accessory board has been designed to implement adjustable signal conditioning for the Alpha250. This board includes:

- Variable gain amplifiers (VGA) and offsets for the slow analog inputs and outputs allowing up to ±10 V signal compliance
- Variable gain amplifiers for the main ADCs
- Fixed 20 dB amplifiers for the main DACs
- One ±100 V High Voltage amplifier

On the processor side, an Ubuntu Linux operating system runs and manages all the FPGA registers, a web server and the software for additional features as the Auto-Locker. The web server runs a web interface (Fig. 1a) that allows monitoring and control from any PC in the network. The same web server also can accept Python commands. The Auto-Locker algorithm monitors a selectable "locking condition" that can be an input,

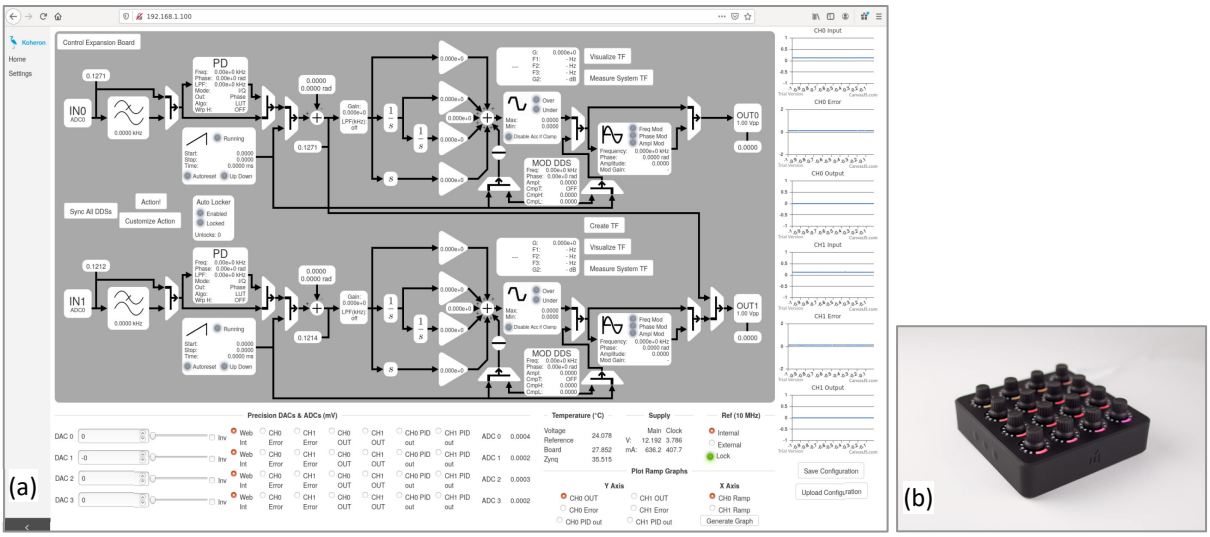

Fig. 1. (a) Web interface to control and monitor the servo. Each block is interactive and allows changes to its configuration and parameters. (b) Picture of the USB rotary knob console used for fine-tuning.

internal signal, or noise level. When the locking condition is not satisfied, the Auto-Locker ramps the output offset of the PIID until the system reacquires lock automatically. The web interface also includes tools to measure, visualize, and optimize the transfer function of the system. To facilitate coarse and fine-tuning of all PIID parameters, support for a USB rotary knob console (Fig. 1b) is implemented. Through a web interface, each of the 64 knobs (16 on 4 different banks) available on the MIDI Fighter Twister console [16] can be mapped to act on any specific parameter in the system.

To demonstrate the low-latency digital servo, we phase-locked a Dielectric Resonator Oscillator (DRO) at 10 GHz with a feedback bandwidth of more than a 1 MHz to a reference DRO, the result is shown in Fig. 2.

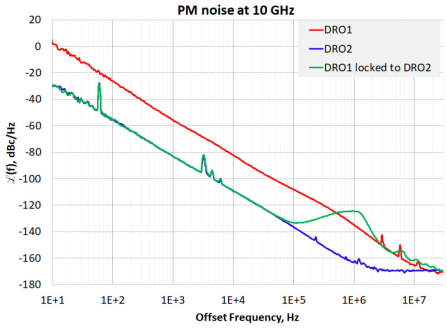

Fig. 2. Two phase-locked DROs at 10 GHz indicating ~1 MHz closed-loop bandwidth of the FPGA-based digital servo.

III. Conclusions

We discussed the features and performance of a FPGA-based digital servo. This servo incorporates a PIID controller along with internal NCOs, PD utilizing a fast I/Q detection algorithm, NCO modulator, network analyzer, auto-locker, ramp generator, and low pass filters. The servo has a minimum latency of 200 ns and closed-loop bandwidth of approximately 1 MHz. We have also successfully implemented this digital servo for PDH lock and for the stabilization of two degrees of freedom of an optical frequency comb.

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