Power Dissipation in a Vertically Integrated Chip-Scale Atomic Clock

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***Abstract*— The physics package of a vertically integrated chip-scale atomic clock based on cesium has recently been demonstrated at NIST. This device requires 69 mW of electrical power to maintain the vapor cell 34 K above the temperature of the baseplate. The physics package structure is analyzed by use of analytical thermal modeling and finite-element calculation. Improvements to the design are proposed to reduce the power consumption of the physics package alone to near 15 mW and of a full chip-scale atomic clock to below approximately 30 mW. Power consumption at this level will open the door to the use of atomic frequency references in portable, battery-operated applications such as wireless communications and global positioning.**

Keywords - Atomic clock, compact frequency reference, CSAC, micromachining, MEMS, VCSEL

I. INTRODUCTION

Compact atomic frequency references based on fabrication techniques used for microelectromechanical systems (MEMS) [1] are rapidly becoming a compelling technological solution to a variety of timing problems arising in applications from wireless communications [2] to global positioning [3] and network synchronization [4]. The use of coherent population trapping to excite microwave resonances in atoms [5][6] and recent advances in alkali vapor cell fabrication using MEMS processes [7][8] have paved the way to the first demonstration of a microfabricated atomic clock physics package [9]. This device, based on Cs atoms, had a volume of 9.5 mm^3 and a short-term fractional frequency instability of 2.5×10^{-10} at one second of integration.

The vertically integrated structure, shown schematically in Fig. 1, allows many physics packages to be assembled simultaneously at the wafer level by means of lithographically-defined arrays of structures [10]. This wafer-level fabrication process will substantially reduce the cost of manufacturing atomic clocks, and may also provide a higher degree of frequency uniformity for devices fabricated on the same set of wafers.

II. POWER DISSIPATION IN THE NIST CHIP-SCALE ATOMIC CLOCK

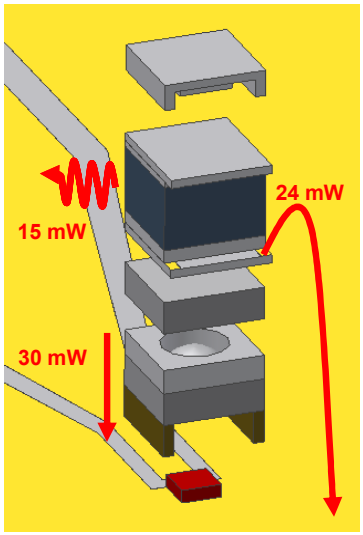

Fig. 1 Power dissipation in the first, cesium-based chip-scale atomic clock developed at NIST. Thermal modelling indicates that roughly 30 mW are dissipated by conduction through the support structure and 24 mW are dissipated by conduction through the wire bonds. The remainder of the 69 mW measured is presumably lost through radiation, and convection and conduction through the air surrounding the package.

The electrical power required to run the physics package, not including the base-plate heating, was 75 mW and was dominated by the power required to heat the cell. A total of 69 mW was required to heat the cell to 80 ºC, 34 K above the baseplate temperature of 46 ºC. The baseplate temperature was maintained above ambient in order to tune the laser wavelength to the Cs atomic transition. This elevated baseplate temperature is not generally required to run the physics package, and the power used to heat the baseplate is therefore not included in our evaluation of the power dissipation. By modeling the heat flow in the structure, both analytically and with a finite-element computation, the heat loss channels could be roughly identified. We estimate that 30 mW is lost through the lower spacer unit, and that 24 mW is lost through the six gold wire bonds, each of diameter 25 μm and length ~2 mm, providing the electrical

connections to the baseplate. The remainder is presumably lost through radiation, and through conduction and convection in the air surrounding the physics package.

III. Improvements in Thermal Design

Significant improvements in the thermal engineering are still possible and promise to reduce the power required to heat the cell to near 10 mW. The main sources of heat loss are conduction from cell to baseplate through the lower spacer unit and the wire bonds, conduction to the air surrounding the package, and radiation. Conduction to the air surrounding the package could be reduced to a negligible level by packaging the physics package in a vacuum enclosure, as shown in Fig. 2. If the gas pressure in the evacuated enclosure were significantly below ~ 1 Pa, the thermal conductivity should be negligible. Heat loss due to radiation between the cell and the shield is given by the Stefan-Boltzmann law,

$$\dot{Q} = \alpha\sigma\left(T_1^4 - T_0^4\right)A \ , \qquad (1)$$

where α is the emissivity of the surface material, σ is the Stefan-Boltzmann constant, A is the area of the radiating surface, and T_1 and T_0 are the temperatures of the cell and surroundings respectively. If a gold coating, with emissivity 0.02, were placed on the interior surface of the shield, the heat loss due to radiation would be roughly 0.1 mW for a temperature difference of 50 K.

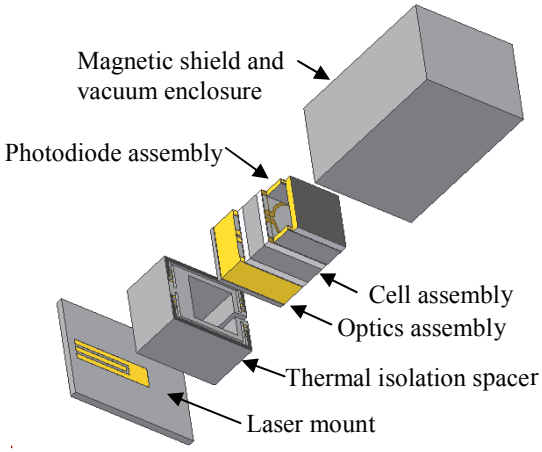

Fig. 2 Advanced thermal isolation using a low-conductivity thermal isolation spacer (see expanded view in Fig. 3) and vacuum packaging of the cell sub-assembly.

Thermal conduction between the cell and the baseplate will be addressed with an advanced design for the thermal isolation spacer. The first modification to the existing spacer will be to use a material with a lower thermal conductivity. Pyrex has a thermal conductivity of 1.4 W/(m•K), while some polymer materials such as Teflon or SU-8 photoresist have thermal conductivities in the range of 0.2 W/(m•K), allowing reduction by a factor of 7 in the power required to maintain a given temperature difference. For a spacer of height 1 mm and with walls of thickness 0.1 mm supporting the structure on its outside edges, the expected power dissipation is 6 mW for a temperature difference $(T_1\text{-}T_0)$ of 50 K, based on the equation

$$\dot{Q} = I(T_1 - T_0)\frac{A}{L}. \qquad (2)$$

Here I is the thermal conductivity of the material, A is the material's cross-sectional area and L is the material length along the direction of heat flow. A more careful analysis of the structure shown in Fig. 3 indicated a power dissipation of 7.2 mW to maintain a ΔT of 50K

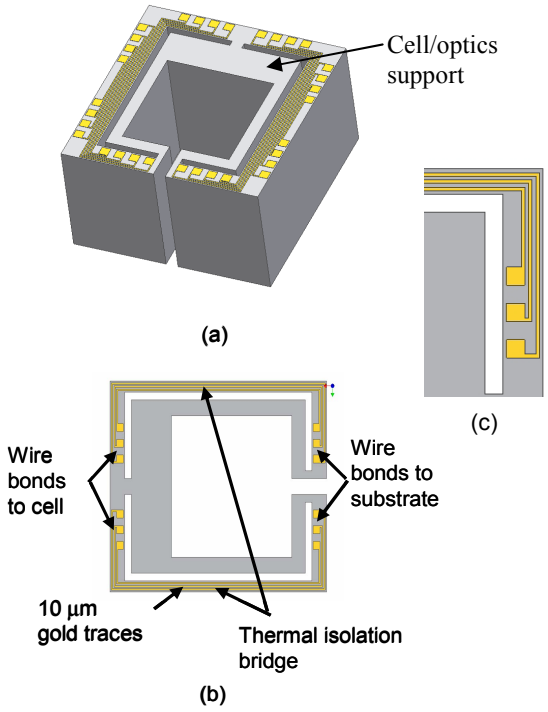

Fig. 3 Thermal isolation of electrical connections from cell to baseplate. Thin gold traces, 10 µm wide are patterned on the top surface of the spacer. Wire bonds from the cell are connected to one end of the traces, and wire bonds to the baseplate are connected to the other end of the traces. The small cross-sectional area of the gold traces reduces the heat conduction. (a) Iso-view, (b) top view, (c) expanded top view portion.

A single gold wire bond of diameter 25 µm and length 1 mm requires 8 mW to support a temperature difference of 50 K between its ends. Clearly some way of addressing the heat flow through the electrical connections to the cell is needed. Our proposal is to use thin gold traces patterned on the top surface of the spacer to provide the thermal isolation. A diagram of how this might work is shown in Fig. 3. Gold traces of width 10 µm, thickness 2 µm and length 1 mm would have a heat dissipation of 0.3 mW/trace for a ΔT of 50 K between the trace ends. Thus, six traces would be expected to

dissipate about 1.8 mW of power. The additional cross-sectional area of the spacer needed to support the traces would dissipate roughly an additional 2 mW. Thus the total expected power dissipation to support a ΔT of 50 K with both the advanced spacer unit and vacuum packaging is expected to be about 11 mW. Finite-element analysis of the CSAC power dissipation yields similar results, as shown in Fig. 4.

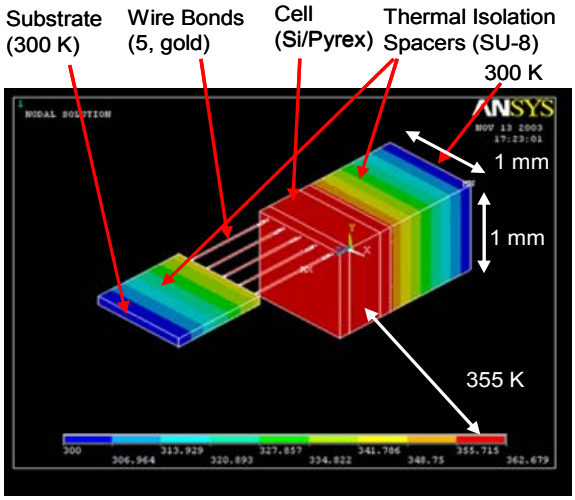

Fig. 4 Finite-element thermal analysis of an advanced CSAC structure. Here a total of 5 mW of thermal power is input to the two faces of the cell, which is isolated from the baseplate by a thermal isolation spacer made from a polymer material. The gold wire bonds are also thermally isolated in a manner similar to that described in Fig. 3. A temperature 55 K above ambient is achieved. Radiative losses are also included.

IV. The Laser Heat Dissipation Problem

In addition to the power dissipated to heat the cell, the physics package has one other important component that dissipates power. The laser DC power dissipation is about 4 mW at the current used here, and the RF power required to modulate the laser at 4.6 GHz is 70 µW. The laser power consumption is unique in that (a) most of the power must be dissipated as heat by the structure supporting the laser, and (b) the laser must be operated at a constant temperature and injection current in order to maintain a constant optical field intensity inside the cell and reduce time-varying AC Stark shifts of the clock output frequency. We propose to maintain the laser at a constant temperature by using a small heater directly under the laser. However, the laser will be heated by its own power dissipation even with no power input from the heater.

We assume that the ambient temperature can be in a range from T_{min} to T_{max}, and that the laser is kept at a constant temperature $T_L > T_{max}$. If the thermal conductance between the laser and the environment is constant, and it is assumed that no heater current is used to heat the laser when $T_{ambient} = T_{max}$, then the power required to heat the laser when $T_{ambient} = T_{min}$ is given by

$$P_{\max} = \frac{(T_L - T_{\min})}{(T_L - T_{\max})} P_{\min}, \qquad (3)$$

where P_{min} is the power dissipated by the laser alone. This implies that if P_{min} = 4 mW, T_{min} = –40 ºC, T_{max} = 60 ºC and T_L = 80 ºC, then the maximum power dissipation P_{max} = 24 mW. Because of the large power dissipated at the minimum ambient temperature, it is clear that this design is not ideal and that the laser should probably be thermally connected to the cell in order to use the power dissipated by the laser to heat the entire physics package. If this is done, Eq. (3) describes the maximum power required to heat the physics package, and not just the laser. There are several other approaches that will help address this difficulty. One is to increase the operating temperature of the laser while simultaneously decreasing the thermal conductance between the laser package and the environment. A second is to reduce the power dissipated by the laser, by running it close to threshold, for example.

V. Overall Power Budget

The power required to provide a longitudinal magnetic field and sense the cell temperature should be well below 1 mW in the final design. With a total of 15 mW projected for the physics package, 15 mW remain for the local oscillator and control circuitry. The control circuit being developed by NIST, in its current design, is based on a small, low-power microprocessor. Running at 3 MHz, this processor should be able to implement all the CSAC control circuits with a power dissipation of 4.5 mW. This leaves 5 mW for the local oscillator, which should be sufficient, given the LO phase noise requirements [11] and 3.6 mW for the frequency divider needed to generate an output near 10 MHz. A summary of the final CSAC power budget is outlined in Table I.

TABLE I. Estimated Power Budget for an Advanced Chip-Scale Atomic Clock

Component	*Power*	*Confidence*
Heating of cell (modeling):	11.1 mW	high
Diode laser DC power (measured):	4 mW	high
Diode laser RF power (measured):	70 µW	high
Local oscillator (estimate):	5 mW	low
Control circuit (MPU, 3 MHz):	4.5 mW	moderate
Frequency divider	3.6 mW	low
B-field, temperature sensor, etc. (est.):	< 1 mW	high
Total	**29.3 mW**	**moderate**

Acknowledgments

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