A low noise 100 MHz distribution amplifier for precision metrology

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Abstract

We have realized a new distribution amplifier with 0 dB direct gain. The amplifier handles up to 13 dBm at 100 MHz with low harmonic distortion and has a reverse gain smaller than -100 dB. The input and output return losses are tipically more than 25 dB. Each channel consists of one common collector NPN and two common base PNP BJT stages with a channel current of 40 mA. The power dissipation is approximately 1 W/channel using a 20 V single supply. A white PM noise floor of $S_\phi(10\,\mathrm{kHz}) = -173\,\mathrm{rad}^2\,\mathrm{Hz}^{-1}$ and flicker phase noise of $S_\phi(10\,\mathrm{Hz}) = -163\,\mathrm{rad}^2\,\mathrm{Hz}^{-1}$ have been measured. We have also measured a temperature coefficient of phase delay smaller than 0.4 ps/K. Circuit design phylosophy and performances will be described in detail.

1 Introduction

Distribution amplifiers are widely used in measurement systems to create independent copies of reference signals, as show in Figure 1.

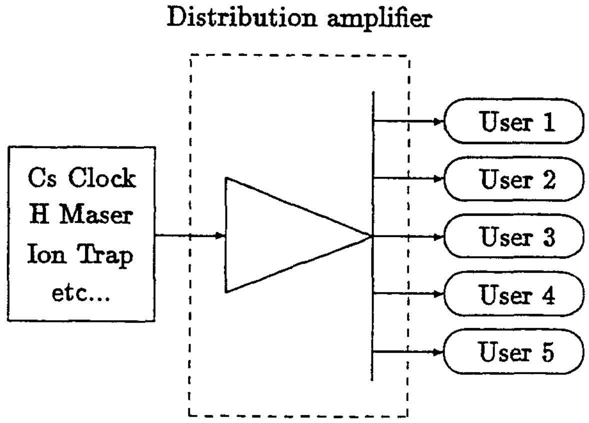

Figure 1: Distribution amplifier operation.

Basic characteristics of this device are high outputs-to-input isolation and negligible crosstalk between outputs. Low phase noise, low distortion, good impedance match and low environmental sensitivities are required [1]. In addition, it is necessary to preserve spectral purity characteristics of distributed signals. Finally, low power dissipation is necessary for distribution system with multiple channels.

Distribution amplifiers suitable for 5 MHz to 10 MHz applications were reported in [3]. New distribution amplifiers for 100 MHz applications are now required by research laboratories to improve timing and frequency accuracy. The advantages of an increase in reference signal frequency in measurement systems are show in [1].

We have made a 100 MHz distribution amplifier with unitary gain, high linearity and low distorsion for input powers up to 13 dBm. The circuit design philosophy follows the same guidelines successfully used for similar devices [2][3], in which the signal is carried by current through a high isolation chain made by common-base BJT

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stages. Each chain is completed by input and output stages to build an isolating channel. A distribution amplifier is obtained by connecting channels in parallel.

2 The isolation channel

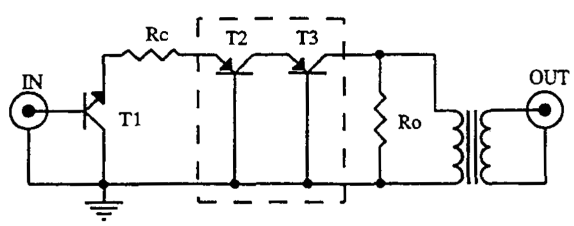

Figure 2: Basic structure of a channel.

The channel structure is shown in Figure 2. A chain of two common base BJT stages, T_2 and T_3, is current driven by the common collector BJT voltage buffer T_1 and the resistor R_c. R_c operates like a voltage to current converter. The chain made by T_2 and T_3 is a unidirectional current buffer. Its direct gain is almost unity and its reverse attenuation is very high. Resistor R_o converts the collector current of T_3 which is the chain output current, into voltage. The chain current gain is almost unity. Finally the output match is made by a transformer.

The use of BJTs with $f_T > 4$ GHz, at the operating frequency of 100 MHz, and a DC current of approximately 40 mA yields a theoretical channel reverse gain smaller than -120 dB in our configuration. This derives from the very small capacitive coupling between collector and emitter, the low impedance due to the high standing current, and the shielding between collector and emitter due to the grounded base configuration of T_2 and T_3. To improve ground connection efficency, low base resistance BJTs were used.

The common collector input stage makes the channel input impedance independent of the amplitude of the current signal going to the isolation chain. The channel input impedance has a design value of 250 Ω in order to set the device input impedance to 50 Ω. The voltage-to-current conversion network is made by the series of buffer (T_1) output impedance, resistor R_c and chain (T_2) input impedance. The latter is a function of quiescent current inside BJT T_2 and it can be viewed as a virtual short to ground. The voltage buffer output impedance is a function of the quiescent current inside T_1 and can be neglected. An admittance of 20 mS is required to obtain a 20 mA rms chain current from an input signal of 13 dBm.

The value of resistor R_o (200 Ω) and the transformer ratio (2 to 1) allow a theoretical output signal of 13 dBm for the nominal input power. Impedance match of the output is also obtained by this approach.

Signal losses in BJTs and transformer are compensated by increasing the value of resistor R_o to 302 Ω. The result is a channel gain of 0 dB and output match to 50 Ω.

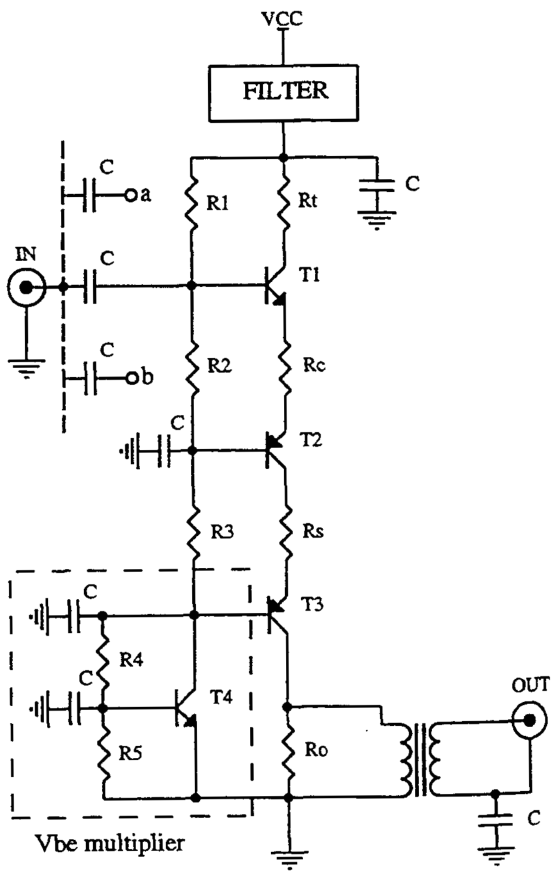

Figure 3: Schematics of a biased channel: on the dashed line more channels can be connected in parallel. As an example 'a' and 'b' can be viewed as the channel entry point (after the input's capacitor) for two of these.

By choosing an NPN BJT for T_1 and a PNP BJT for T_2 and T_3 the channel is biased by a single primary current that flows through all active devices, as shown in Figure 3. This current starts from a positive voltage supply and ends at ground. In this way the output stages are not connected to any DC supply. Consequently the channel-to-channel crosstalk through supply lines is greatly reduced.

The quiescent current coming from the isolation chain is grounded by the primary winding of the output transformer. This reduces the DC voltage needed at the collector of T_3 to avoid cutoff when the load is open and hence reduces the power dissipation. As a result, harmonic distortion may be introduced due to saturation in the transformer's core by high values of DC current. Thus, the harmonic distortion is increased by increasing DC current. On the other hand, the BJTs quiescent collector current must be greater than the peak signal current. The harmonic distortion due to the non-linear behavior of BJTs increases by decreasing the quiescent current. Measurements on our particular choice have shown that a quiescent current of 38 mA DC minimizes the global harmonic level functions, which therefore is the design value.

The ratio of bias voltage across emitters of T_1 and T_2 and value of the resistor R_c set the primary quiescent current. This current changes with emitter bias voltage due to the dispersion of h_{fe} values in BJTs. To reduce this problem a V_{be} multiplier is used instead of a classical resistor to connect the base of BJT's T_3 to ground. The V_{be} multiplier is realized by transistor T_4. This approach decreases the current dispersion from channel to channel to less than 5%.

To avoid possible DC ground loops in measurement systems that include this device, the output ground is connected only by capacitor to the device main ground.

3 Realized devices and measurements

A distribution amplifier is made by connecting the inputs of several isolating channels in parallel. The input impedance of the device is, therefore, the parallel of several channel's input impedances. Different versions with different number of channels were made. In devices with a number of channels lower than five, a shunt resis-

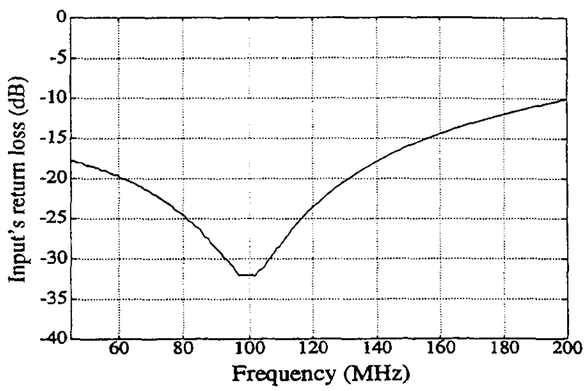

Figure 4: Plot of the device's input return loss.

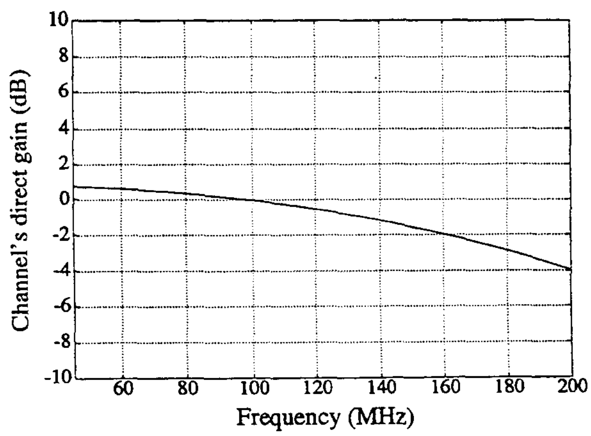

Figure 5: Plot of a channel's direct gain.

the omitted channels.

The reverse channel gain at 100 MHz is smaller than -100 dB. Channel to channel crosstalk is smaller than -100 dB.

Harmonic distortion is -37 dBc at 200 MHz and -40 dBc at 300 MHz.

Phase noise was measured with a crosscorrelation technique [4]. The noise of the measurement system was always 5 dB below the noise in measured devices.

Measurement results are shown in Table 1. The phase delay change with temperature was

$f(Hz)$	10	100	1000	10000
$S_\phi(\mathrm{rad^2\,Hz^{-1}})$	-163	-170	-172	-173

Table 1: Phase noise at different Fourier frequency.

about 0.3 ps K^{-1}.

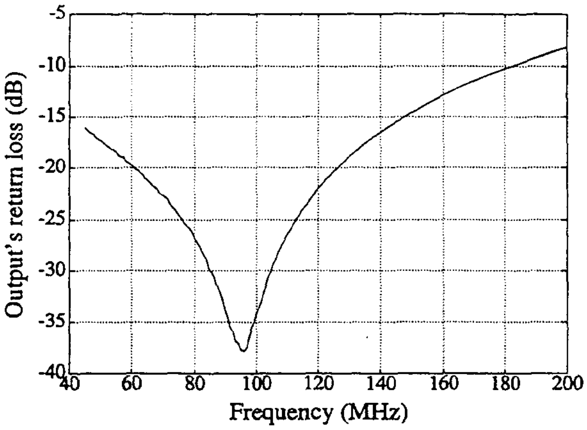

Figure 6: Plot of a channel's output return loss.

The measurements of the scattering parameters are shown in Figure 4, 5 and 6.

4 Conclusion

Measurements show exellent phase noise, isolation, and temperature coefficient of phase delay for the new 100 MHz distribution amplifier. The philosophy of carrying signal via current seems to be a winning way for designing distribution amplifiers [3][2].

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