A DIGITAL 5.00688 MHz SYNTHESIZER AND SQUAREWAVE FM SERVO SYSTEM FOR CESIUM STANDARDS

David A. Howe and Henry F. Salazar

Time and Frequency Division
National Bureau of Standards
Boulder, Colorado, 80302

ABSTRACT

The cesium clock transition is at 9, 192, 631, 770 Hz by definition. In the design of a cesium frequency standard, it is common to generate a 5-MHz signal which is locked to this transition. Since 5-MHz cannot be directly multiplied to match the exact clock transition frequency, usually another frequency is synthesized and mixed in such a way that the clock transition frequency is produced.

This paper describes a synthesizer using a 5-MHz reference which has an output frequency of 5.00688 MHz which is very nearly an integer submultiple of the cesium clock transition frequency. Indirect synthesis is used in which an internal (number controlled) oscillator is locked at a prescribed frequency offset relative to the reference. Resolution (quantization error) is 1.4 parts in 10^{13}. A frequency stability plot $\sigma_y(\tau)$ of the synthesizer noise is presented. The synthesizer can be made very compact and reliable. Since its output has low phase noise, the signal may be multiplied directly to the cesium clock transition frequency. In a cesium standard, this simplifies the amount of microwave hardware compared to traditional schemes. The design concepts of the synthesizer can easily be extended in order to implement squarewave frequency modulation of the beam tube RF excitation.

INTRODUCTION

It is desirable in a Cs frequency standard to generate the clock transition frequency of 9.192... GHz with low phase noise. This is essential in order to make the servo system correctly lock an oscillator to the Ramsey-line center. In order to minimize X-band phase noise and lock a 5-MHz oscillator, the scheme shown in Fig. 1 has been adopted in many cases. A low noise 5-MHz VCXO is multiplied to 9.180 GHz and mixed with a 12.632 MHz signal synthesized from the 5 MHz oscillator. The advantage to this scheme is that the synthesizer noise component is added at X-band. This means that the requirement for low synthesizer phase noise is relaxed. The VCXO noise component is multiplied by 1836, so it must be made sufficiently small using a high quality oscillator. The noise contribution due to the multiplier can likewise be made small [1].

In an attempt to simplify the scheme of Fig. 1, we pursued an alternate approach. If one could synthesize 5.00688 MHz, a submultiple of 9.192... GHz, using 5-MHz as a reference, then the microwave mixer and filter could be eliminated. Furthermore, one could then synthesize [5.00688 + δf]MHz and [5.00688 - δf]MHz where δf is half the Ramsey linewidth. If the switch from +δf to -δf were made at a constant rate, then one would have square wave frequency modulation of the Ramsey line. The 5-MHz reference could then be servoed by a lock-in amplifier connected to the beam tube detector. This approach is shown schematically in Figure 2. In implementing this technique, it is essential that the synthesizer output have low phase noise since it is multiplied by 1836 [2]. Also, its resolution must be high in order to interrogate the Ramsey line with good precision. The important distinction between Fig. 1 and Fig. 2 is that one requires a low-noise oscillator and the other requires a low-noise synthesizer.

There are two basic snythesizer designs: direct and indirect. Direct frequency synthesizers require high-density read-only memories and very fast digital-to-analog converters to obtain low phase noise [3]. Indirect synthesizers utilize an internal oscillator which is locked to a reference signal according to:

$$f_{synth.osc.} = \frac{A}{B} \cdot f_{ref.}$$

In a digital synthesizer, A and B are integers. The ability to lower the phase noise of the locked oscillator relative to the reference depends upon the sample rate obtained for particular values of A and B. The degree to which the locked oscillator degrades goes as the sample rate. It is possible to maximize the sample rate over a wide range of synthesizer frequencies by using several locked oscillators and mixing them [4].

We have developed a method of locking a 5.00688 MHz VCXO at a prescribed offset relative to a 5-MHz oscillator. Resolution of the locking circuitry is better than the stability of the best available quartz oscillators for sample times of 1s and longer. Work has been done previously on a method of locking a 5.00688 MHz oscillator at a programmed offset relative to a 5-MHz reference [5]. The emphasis of this paper is on a new indirect synthesis design.

SYNTHESIZER DESIGN

A block diagram of the synthesizer is shown in Fig. 3. The 5-MHz reference f_r is heterodyned with VCXO f_1, which is at 5.00688 MHz. The resultant 6.88kHz beat note is then mixed against $f_r \div 726$. The final beat frequency f_b is nominally 7 Hz. By producing a low frequency beat note from two relatively high frequency oscillators one is able to measure small fractional frequency fluctuations using a time interval counter with 100 ns resolution. Thus,

$$\frac{\delta\tau_k}{\tau_k} = \frac{\delta f_1}{f_b} \cdot = \left[\frac{f_1}{f_b}\right] \frac{\delta f_1}{f_1} .$$

where $\tau = \frac{1}{f_b}$ and τ_k is the k^{th} period corresponding to f_b.

We see that fractional frequency fluctuations $\frac{\delta f_1}{f_1}$ are multiplied by the ratio of f_1 to f_b in

order to obtain fractional period fluctuations $\frac{\delta\tau_k}{\tau_k}$ of the beat note. The period, τ_k, is measured by a time-interval counter using a 10-MHz time-base reference f_c which can be conveniently derived from the 5-MHz reference. A feedback loop locks the period of the VCXO to a desired value $N\tau_b$ which is an integer number of period of f_b and is the gate period for the time interval counter (τ_b = 143 ms). Thus,

$$\tau_k = N\tau_b\left(1 + \frac{\delta\tau_k}{N\tau_b}\right) = N\tau_b\left(1 + H\frac{\delta f_{1,k}}{f_1}\right)$$

where $H = \frac{f_1}{f_b}$.

The counter generates a number x_k at the end of interval τ_k given by

$$x_k = f_c\,\tau_{k-1}.$$

The counter output x_k is then subtracted from a preset number x^* which is related to τ_b by:

$$x^* = f_c N\tau_b.$$

And the output of the subtractor, denoted by "$\overline{X}_k$", is simply

$$\overline{X}_k = x^* - x_k.$$

An accumulator computes the sum of the $\overline{X}_k$'s, and $\sum\overline{X}_k$ is converted to a voltage through a digital-to-analog converter with a gain constant k_1. The output of the DAC is connected to the varactor control of the 5.00688 MHz VCXO. The frequency of the VCXO is related to the voltage applied to its varactor by gain constant k_2.

The feedback loop applies a correction voltage to the VCXO until $x_k = x^*$, hence $\overline{X}_k = 0$. Referring to Fig. 3, one can break the feedback circuit at M and analyze the open-loop characteristics. At M, we have

$$v_{f_{1,k}} = k_1\sum_{i=0}^{k}\overline{X}_i = k_1\sum_{i=0}^{k-1}\overline{X}_i + k_1\overline{X}_k$$

and therefore $\delta v_{f_{1,k}} = k_1\overline{X}_k$

where $v_{f_{1,k}}$ is the control voltage to the VCXO and $\delta v_{f_{1,k}}$ is the change in v_{f_1} due to $\overline{X}_k$.

$$\overline{X}_k = x^* - x_k = x^* - f_c\,\tau_{k-1}$$

$$= x^* - f_c\left[N\tau_b\,(1 + H\frac{\delta f_{1,k-1}}{f_1})\right]$$

$$= x^* - f_c N\tau_b - (f_c N\tau_b H)\frac{\delta f_{1,k-1}}{f_1}$$

and $$x^* - f_c N\tau_b = 0$$

The maximum resolution of $\frac{\delta f_{1,\,k-1}}{f_1}$ is its deviation when $\Delta\overline{X}_k$ = one unit. This is also known as the quantization error q when dealing with a digital system. We have

$$q = \frac{1}{f_c N\tau_b H}$$

For the system described in Fig. 3:

$$f_c = 10^7 \text{ Hz},$$

$$N\tau_b = 1 \text{ s (7 samples since } \tau_b = 143\text{ms}),$$

and $$H = \frac{5 \times 10^6}{7} = 7.14 \times 10^5.$$

Therefore

$$q = 1.4 \times 10^{-13} \text{ at 1s.}$$

This result means that the smallest fractional frequency fluctuation to which the loop is sensitive will be 1.4×10^{-13} at 1s counter gate interval. The value for τ_b is 143 ms since that is the period of f_b and the counter is gated by zero-crossings of the voltage of f_b (or integer multiples thereof). Increasing f_c lowers q, so it is possible to increase the resolution in $\frac{\delta f_{1,k-1}}{f_1}$ by going to a higher clock rate. It should be noted that time-interval counters can be built with clock rates approaching 1 GHZ. With such speeds, q would approach 1.4×10^{-15} at $N\tau_b$ = 1s.

CLOSED LOOP TIME RESPONSE

At M, we have

$$\delta v_{f_{1,k}} = k_1(f_c N\tau_b H)\,\frac{\delta f_{1,k-1}}{f_1}$$

Now let us close the feedback loop and make the connection at M to the varactor control of the VCXO. Assume that the varactor voltage linearly controls frequency f_1 within a given range such that

$$\Delta f_{1,k} = k_2 v_{f_{1,k}}$$

A fractional frequency change due to $\delta v_{f_{1,k}}$ at M is given by

$$\frac{\delta f'_{1,k}}{f_1} = \left[\frac{k_2}{f_1}\right] \delta v_{f_{1,k}} \text{ and hence}$$

$$\frac{\delta f'_{1,k}}{f_1} = -\frac{k_1 k_2}{f_1} f_c N \tau_b H \frac{\delta f_{1,k-1}}{f_1} = A \frac{\delta f_{1,k-1}}{f_1}$$

This equation describes the action of the loop from the k - 1 sample to the k^{th} sample. If we make the coefficient A = 1 by an appropriate choice of k_1 and k_2, then a fractional frequency fluctuation induced by the feedback loop at the k^{th} sample will be equal in magnitude and opposite in sign to a sensed fractional frequency fluctuation at the k - 1 sample.

The time response of the loop can be studied by plotting the frequency of the VCXO as a function of time or sample number k. Let us assume that the VCXO and reference are noiseless. If the reference frequency, f_r, is stepped at time k = 1 and if A = 1, then we have the following sequence:

$$f_{1,} = k_1 k_2 \left[\bar{X}_o + \bar{X}_1\right] \text{ where } \bar{X}_1 = 0$$

$$f_{1,2} = k_1 k_2 \left[\bar{X}_o + \bar{X}_2\right]$$

$$f_{1,3} = k_1 k_2 \left[\bar{X}_o + \bar{X}_2 + \bar{X}_3\right] \text{ if A = 1, then } \bar{X}_3 = 0$$

$$f_{1,k} = k_1 k_2 \left[\bar{X}_o + \bar{X}_2\right] \quad k > 3$$

If A = 1, then the frequency f_1 of the VCXO is solely determined by the initial value in the accumulator $\bar{X}_o$ and the amplitude $\bar{X}_2$ due to the step at k = 1. This is because $\bar{X}_k = 0$ for k > 2. If A ≠ 1, then $\bar{X}_k \neq 0$ for k > 2, and f_1 is determined by new values in the accumulator at successive k samples.

closed loop time response to a step function is shown graphically in Figure 4 for different values of A. To minimize transient response errors and obtain best tracking and acquisition properties for the loop, the hardware realization of this synthesizer should be such that A = 1.

FREQUENCY DOMAIN CONSIDERATIONS

In order to gain insight into the frequency domain characteristics of the synthesizer we will examine the power spectrum of the error correction signal in the feedback loop for the case where f_r is perturbed by white noise. Referring to Fig. 3, one can derive the following five expressions:

1. $\bar{X}_k = \frac{2f_{r,k-1}}{[f_{1,k-1} - \alpha f_{r,k-1}]}$ where $\alpha = 1 + \frac{1}{726}$

2. $V_k - V^*_{k-1} = \delta V_k = k_1 \bar{X}_k$ where V is voltage out of the DAC

3. $f_{1,k} = f_{1,0}\left(1 - \frac{k_2 V_k}{f_{1,0}}\right)$

4. $f_{r,k} = f_{r,0} + \delta f_{r,k}$

5. $f_{1,k} = f_{1,0} + \delta f_{1,k}$

From these one can derive an expression for changes in $\bar{X}$ as a function of changes in δf_r:

$$\bar{X}_k + 2 f_r k_1 k_2 \bar{X}_{k-1} = -2 f_r \alpha (\delta f_{r,k-1} - \delta f_{r,k-2})$$

We see that a change in $\bar{X}$ over an interval k is due to a change in δf_r over the interval k-1. Let us now make the changes in δf_r a white noise process, that is:

$$S_{\Delta\delta f_r}(f) = \sigma_o^2$$

The resultant power spectrum of changes in X_k is then given by [6],

$$S_{\Delta\bar{X}_k}(f) = \frac{8 f_r^2 \alpha^2 \sigma_o^2 e^{-\pi(fN\tau_b - \frac{1}{2})} \sin^2 \pi f N \tau_b}{(1+\underbrace{2f_r k_1 k_2}_{\beta} \cos 2\pi f N\tau_b)^2 + (2 f_r k_1 k_2 \sin 2\pi f N \tau_b)^2}.$$

The coefficient β governs the behavior of the loop to a high degree. The power spectrum of ΔX_k for different values of β is shown in Fig. 5. For values of β approaching one, we see that the loop becomes unstable at frequencies near one-half the sample rate (the Nyquist frequency). Lower values of β yield more desirable loop behavior with greater power showing up at low Fourier frequencies. Fig. 5 shows that the spectrum goes to zero at f = 0 In the time domain, this means that the variance of fractional frequency differences between f_1 and f_r should decrease for longer averaging times.

SQUARE WAVE FM MODULATION

In order to implement square wave frequency modulation of the Cs clock transition,we can build two 5.00688 MHz synthesizers. One can be tuned to the Ramsey center frequency plus a half-linewidth and the other to the center frequency minus a half-linewidth. It is simpler and cheaper, however, to modify our existing scheme such that the VCXO locks at two frequencies symmetrically located about a center frequency. Fig. 6 shows a method by which this may be accomplished. $\bar{X}_k$ is compared to a preset value $\bar{X}^*$ through a second subtractor. The error ε is sent to an accumulator and then to a DAC as in the previous scheme of Fig. 3. During this time, the VCXO varactor is controlled by the

output of this DAC. In order to lock the VCXO to another frequency symmetric about the $\overline{X}_k = 0$ condition, a switch of the VCXO varactor to another DAC is made. At the same time the second subtractor is programmed to add, and its output is sent to an accumulator which sums the errors γ in this mode. To switch from one frequency to another at a constant rate requires that the second arithmetic unit switch between adding and subtracting at a constant rate. Separate accumulators are used for each mode so that at each frequency the feedback varactor voltage will represent a summation over many samples.

It is important to note that the VCXO frequency is independent of varactor characteristics assuming a monotonic voltage vs. frequency. One sees that, with all other things being equal, the magnitude of $\overline{X}_k$ will approach $\overline{X}^*$ the sign of $\overline{X}_k$ will change depending on whether the second arithmetic element is subtracting or adding. Modulation rates up to twice the Nyquist frequency are possible with this scheme. The servo system for locking the 5-MHz oscillator to the cesium clock transition should have a time constant which is at least ten times longer than the modulation rate. This would allow the cesium servo time constant to be of order 1.4s.

TIME-DOMAIN SYNTHESIZER NOISE

The synthesizer shown in Fig. 3 was built for testing. Time-domain stability measurements using the Allan variance were made between a 5-MHz quartz oscillator and the internal 5.00688 MHz VCXO. Fig. 7 shows $\sigma_y(\tau)$ of the two oscillators independently free-running (circles) and with the synthesizer circuit operating (crosses) for τ from 1 s to about 10,000 s. These data were computed by measuring the 7 Hz beat note out of the second mixer in the unlocked and locked conditions. With averaging times of order 1s, we see a small improvement in the relative stability of the two oscillators using the synthesizer. It is important to realize that the synthesizer contributes nothing for averaging times shorter than the sample rate of the time-interval counter. The minimum rate is 143 ms. since that is the period of the beat note. With an improvement in the free-running relative oscillator stability at 1s, we can expect an improvement in stability under a locked condition up to about 1.4×10^{-13} since this is the resolution of the synthesizer circuit. We see a noticeable improvement in stability for longer averaging times with a value for $\sigma_y(\tau)$ of about 2×10^{-14} at τ = 16,000s One would expect that the type of noise contributed by the synthesizer itself is white phase noise, so the intrinsic noise should go as $1/\tau$. The resultant $\sigma_y(\tau)$ depends to a large degree on the free-running stability of the internal VCXO relative to the reference.

CONCLUSION

We have shown that it is feasible to synthesize 5.00688 MHz for use as a direct submultiple of the cesium clock transition. Limitations on the stability of the synthesizer are governed by the stability of the reference and of the free-running stability of the internal VCXO. With a test synthesizer, $\sigma_y(\tau)$ was about 2×10^{-12} for τ = 1s; $\sigma_y(\tau)$ was about 2×10^{-14} for τ = 16,000s. It is possible to improve the synthesizer stability by using a VCXO with better free-running stability up to the resolution of the synthesizer's time-interval counter--1.4 parts in 10^{13} for a sample time of near 1 s. If resolution is the stability limitation, then converting to a time-interval counter with a clock rate of 100 MHz will improve resolution by an order of magnitude compared to our test synthesizer.

Squarewave frequency modulation of the VCXO can be implemented by a straightforward extension of the synthesizer design. This will accomplish squarewave frequency modulation of the Ramsey centerline with the goal of improving stability of the cesium tube servo system by as much as $\sqrt{2}$ overall compared to sinewave modulation. Frequency modulation rates of 7 Hz and lower are realizable.

Except for mixers and buffer amplifiers, the synthesizer uses conventional digital components. This has the advantage of high noise immunity and reliability. From an analytical standpoint, limitations on resolution and stability can be more accurately defined as compared to analog loops. Current integrated circuit technology allows the entire synthesizer minus the VCXO to fit on a 10 x 20 cm printed circuit card. High quality VCXO's are available in volumes as small as 0.5 ℓ.

ACKNOWLEDGMENT

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REFERENCES

1. D. Halford, A. E. Wainwright, and James A. Barnes, "Flicker Noise of Phase in R.F. Amplifiers and Frequency Multipliers: Characterization, Cause, and Cure" (Summary) Proc. 22nd Annual Symposium on Frequency Control, Fort Monmouth, N. J., pp. 340-341, April 1968.

2. F. L. Walls and A. De Marchi, "R.F. Spectrum of a Signal after Frequency Multiplication; Measurement and Comparison with a Simple Calculation," IEEE Transactions on Instrumentation and Measurements, September 1975 (to be published).

3. R. H. Hosking, "Direct Digital Frequency Synthesis," IEEE Intercon Technical Paper, 1973.

4. D. G. Meyer, "An Ultra Low Noise Direct Frequency Synthesizer," Proc. 24th Annual Symposium on Frequency Control, Fort Monmouth, N. J., pp. 209-232, April 1970.

5. D. A. Howe, H. E. Bell, H. Hellwig, and A. De Marchi, "Preliminary Research and Development of the Cesium Tube Accuracy Evaluation System," Proc. 28th Annual Symposium on Frequency Control, Fort Monmouth, N. J., pp. 362-372, May 1974.

6. G.E.P. Box and G. M. Jenkins, Time Series Analysis Forecasting and Control. San Francisco: Holden-Day, Inc., pp. 46-65. 1970.

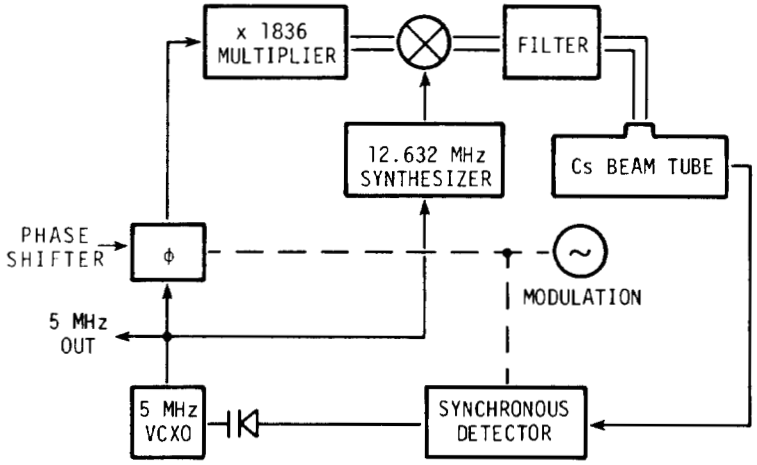

Figure 1. A popular scheme for generating the cesium clock transition frequency is to mix a synthesized 12.632 MHz signal with 9.180 GHz, a multiple of 5 MHz.

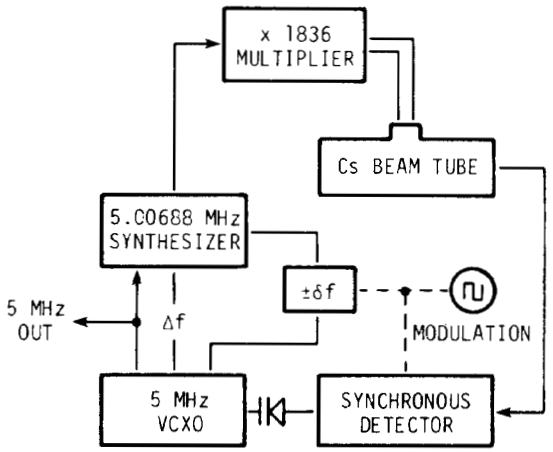

Figure 2. One can eliminate some x-band hardware by synthesizing 5.00688 MHz and directly multiplying to 9.192...GHz

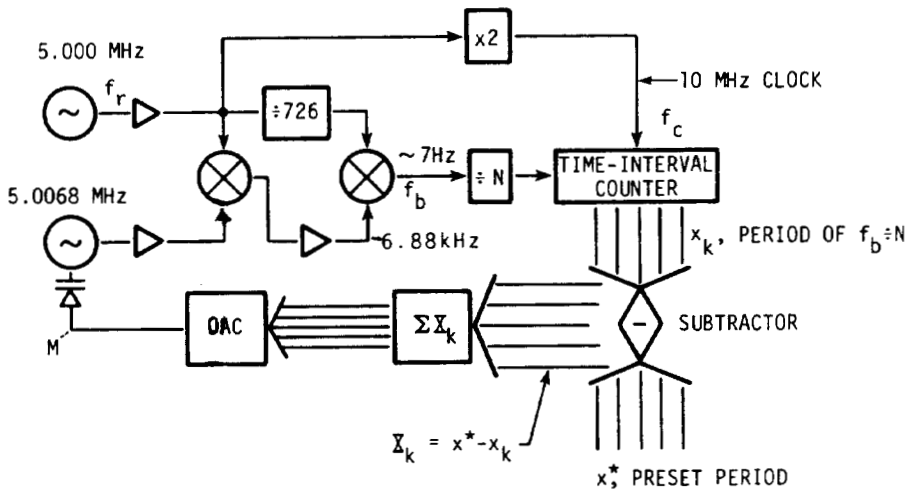

Figure 3. The 5.00688 MHz synthesizer uses a local VCXO. Two mixers and one divider create a low frequency beat note which can be measured using a time-interval counter. A resolution of 1.4 parts in 10^{13} at a 1s gate time is realizable with this scheme.

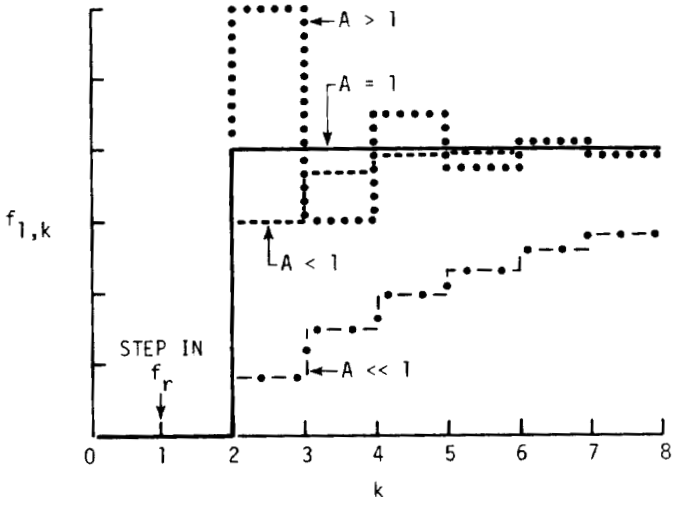

Figure 4. The coefficient "A" given in the test determines the time-response of the loop to a step function.

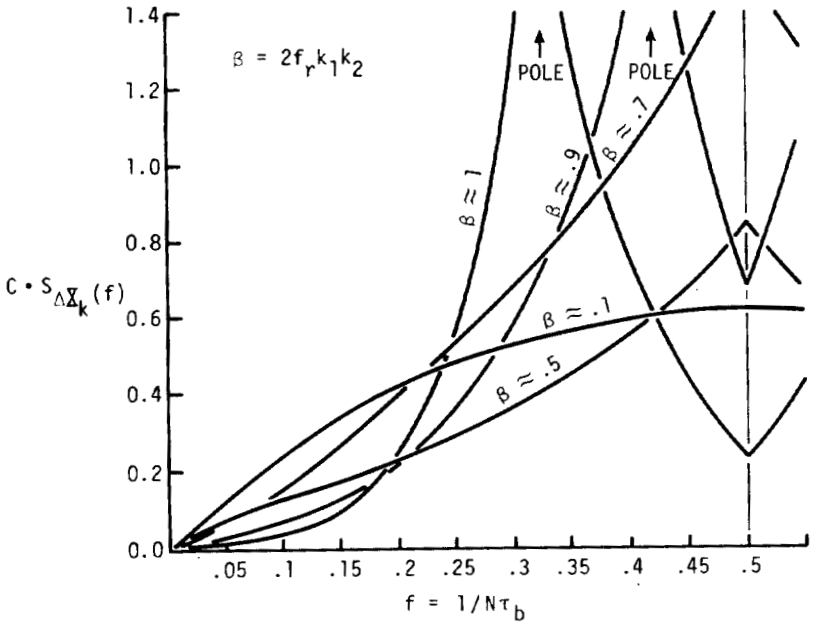

Figure 5. The loop can go into oscillation if the gain constants k_1 and k_2 are too high as shown by the power spectrum of changes in $\Delta\bar{X}_k$.

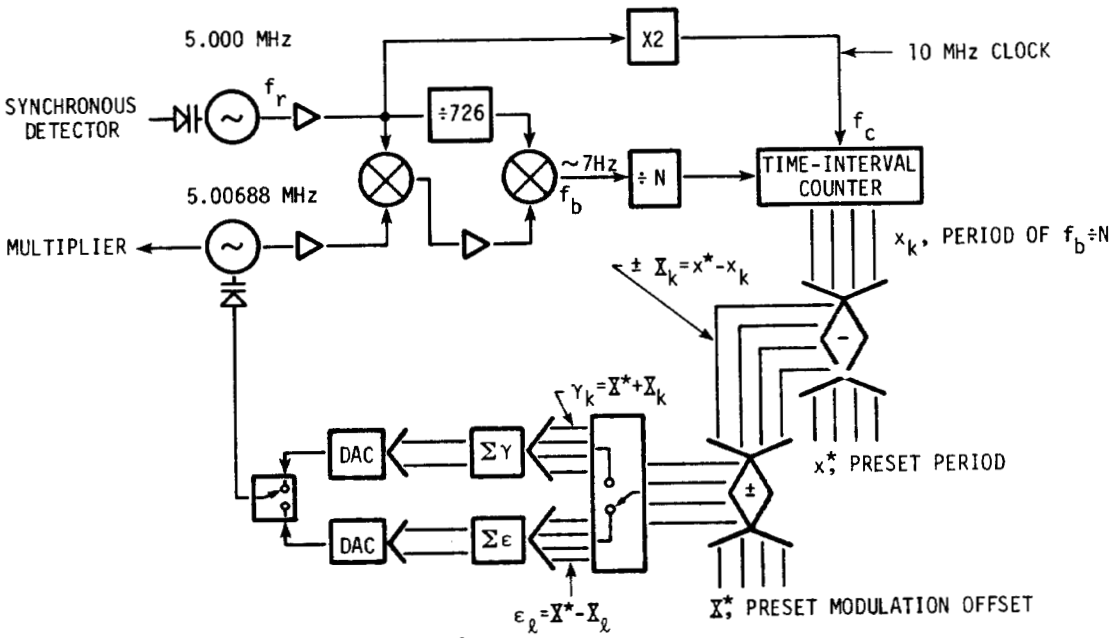

Figure 6. Implementation of squarewave modulation requires the use of an additional arithmetic element, accumulator, and DAC.

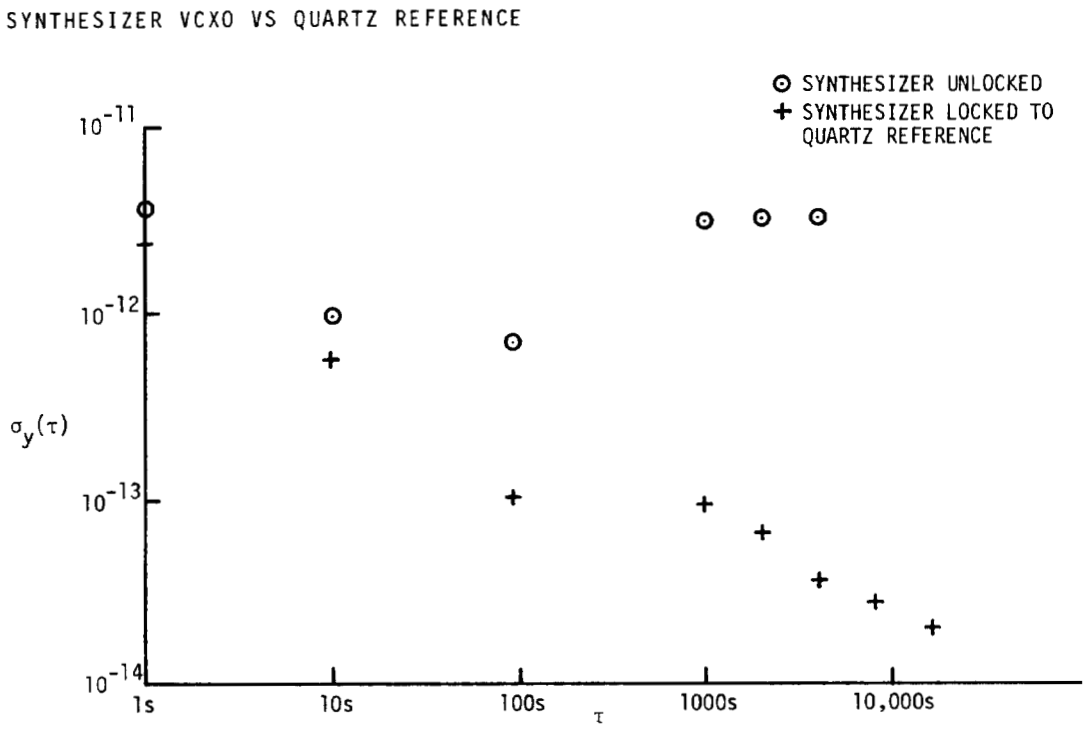

Figure 7. The test synthesizer of Fig. 3 shows a stability of 2×10^{-14} in the locked condition at 16,000 s.