# MICROWAVE SYNTHESISERS FOR ATOMIC FREQUENCY STANDARDS

A. SEN GUPTA', J. F. GARCIA NAVA', C. NELSON', D. A HOWE' and F. L. WALLS' + National Physical Laboratory, New Delhi, India \* National Institute of Standards & Technology, Boulder, Co, USA # Total Frequency, Boulder CO, USA

Following our earlier work on a new approach to synthesising the Cs hyperfine frequency of 9.192 GHz, we describe developments on its further refinements. The salient feature of our design is that it is based mainly on frequency division and requires no narrow band filter stages. Tests indicate an internal fractional frequency stability of  $1.5 \times 10^{-15}$  at 10 s and  $1 \times 10^{-18}$  at 1 day. The temperature coefficient is approximately 0.1 ps to 0.5 ps/K. We have added digital control of the oscillators so that no mechanical tuning is needed over a 25-year lifetime. The unit is powered by 24 ±4 VDC and uses RS 432 for the output frequency and phase control and monitoring functions. We also describe a general design to produce simultaneously outputs of 9.192 GHz for Cs, 6.834 GHz for Rb, 1.42 GHz for H-maser, 40.5 GHz for Hg<sup>+</sup>, 10GHz for femtosecond pulse repetition rate generation, etc. The synthesiser can be phase locked to an external reference of 5, 10 or 100 MHz or a microwave cryogenic oscillator.

### 1. Introduction and Summary

The design details and data on our Cs synthesiser are given in an earlier publication [1]. The novelty of this design is that it is based only on frequency division and mixing and there are no narrow band filters. Proper heat sinking of all parts and simple temperature compensation result in a very low temperature coefficient and hence excellent internal stability, approaching  $10^{18}$  at one day. Following the success of two initial prototypes [1], several more units have been made with some improvements as given in the following.

(1) Use of a single input dc voltage of  $24 \pm 4$  V with dc-to-dc converters to provide the specific voltages needed for different circuits. This makes it easy for batteries and charging circuits to provide failsafe power to the unit for long periods of time. We find that there is a phase shift of approximately 1 ps/V change in the power supply voltage. We have not yet identified which sub system is responsible for this voltage coefficient, however an external supply voltage stability of 0.1 V is readily obtainable.

(2) Implementation of digital control of the coarse tuning of the 100 MHz and 5 MHz oscillators. Previously one had to mechanically tune the oscillators every several years to compensate for long-term drift. This is incompatible with the PARCS (Primary Atomic Reference Clock in Space) mission and in general inconvenient. The dc control should provide tuning over the 25year lifetime of the oscillators.

(3) Use of RS432 lines for all control and monitor functions. This addressable type of serial communications controls the direct digital synthesiser(s) (DDS). The output frequency of the synthesiser can be switched to a new value over a period of 20 ns, which is the period of the DDS clock. It is also possible to make precise changes of the output phase, without any discontinuity, by simply switching the output frequency to a new value any

restoring it after a known multiple of 20 ns. Coarse tuning of the oscillators and monitoring of all the servo voltages is also done over the RS432 lines:

## 2. Design of a more general microwave synthesiser

A novel feature of our approach of frequency synthesis is that it is quite straightforward to simultaneously produce several outputs applicable to other atomic frequency standards. We describe below such a design in block schematic. Fig 1 shows the basic divider unit. It consists of the 6.4 GHz dielectric resonant oscillator (DRO) or Yttrium-Iron-Garnet (YIG) oscillator, which is phase locked to the 100 MHz and 5 MHz quartz oscillators for spectral purity. One could also consider phase-locking the DRO to a microwave reference such as a superconducting cavity oscillator (SCCO) as long as the frequency is within  $\pm$  20 MHz of one of the internal reference frequencies (3.2 GHz, 6.4 GHz, 9.2 GHz, 9.6 GHz, 10 GHz). To achieve this, one could use a phase-locked-loop (PLL) with a DDS set to the difference between the internal reference frequency and that of the SCCO. The output error of this PLL could correct the 6.4 GHz DRO with a bandwidth of up to approximately 300 kHz. The 6.4 GHz output is first divided using a regenerative divider to produce the 9.6 GHz and 3.2 GHz outputs. The 3.2 GHz output is successively divided to 1.6 GHz, 400 MHz, 200 MHz, 100 MHz, 10 MHz and 5 MHz. Presently for our Cs synthesiser, commercially available digital dividers have been used. However, these have the disadvantage of introducing noise floors that compromise the advantage of phase locking with the quartz oscillators and also the low noise floor of the 6.4 GHz oscillator far away from the carrier. Therefore, at a later time it may be worthwhile to use regenerative dividers [2] for the entire divider chain, which incidentally will have the advantage of lower temperature coefficient. Using the basic divider unit one can then generate the various output frequencies as needed.

# 2.1 Cs, Rb and other outputs

Figure 2 shows the scheme for generating the Cs output of 9.192... GHz. This has already been adequately discussed in [1]. Figure 3 shows the scheme for generating the Rb output of 6.834,... GHz. Here we can generate a 34 MHz output by mixing the roughly 9 MHz DDS signal with the 25 MHz derived by dividing the 100 MHz by 4, in an USB mixer. The use of an USB eliminates the need for a narrow band filter to reduce the unwanted 9 MHz side bands. The 34 MHz signal is mixed with 400 MHz in another USB mixer to produce 434 MHz. The 434 MHz is mixed with the 6.4 GHz to give the needed 6.834 GHz output. A 6.834 GHz band pass filter with a width of 180 MHz is used to eliminate the unwanted 434 MHz side bands. In a similar manner it is fairly simple to work out schemes of synthesising other frequencies such as for an H-maser, Hg<sup>+</sup> (40.5GHz), etc.

## 2.2 Femtosecond laser pulse repetition rate (PRR)

Mode-locked fs pulse lasers provide ultra-short pulses (~30 fs) at the pulse repetition rate (PRR). This is typically 100 MHz to a few GHz. This modulation yields a comb of frequencies extending up to optical frequencies. Mode-locked fs lasers have been used to make frequency comparisons between the PRR or multiples of the PRR and optical

frequencies with unprecedented precision and accuracy [3]. Readily available frequencies out of our synthesiser for fs pulse PRR could be 10.0, 9.6, 9.2, 6.4, or 3.2 GHz.



Figure 1. Basic oscillator, phase locked loops and divider chains in the proposed synthesiser



Figure 2. Synthesis scheme for producing output frequency corresponding to Cesium



Figure 3. Synthesis scheme for generating the output frequency corresponding to Rubidium

### References

- 1. Sen Gupta A., D. Popovich and F.L. Walls, IEEE Trans UFFC, 47, Mar 2000, p 475-479
- 2. M. Mossammaparast et al, Proc. 2000 IEEE/EIA Intl, Freq. Control Symp, pp 531-535
- 3. Yun Ye et al, Optics Letters, 25, pp. 1675-1677, 2000

#### Acknowledgements

One of us (ASG) would like gratefully acknowledge funding support under the Indo-US collaboration program.